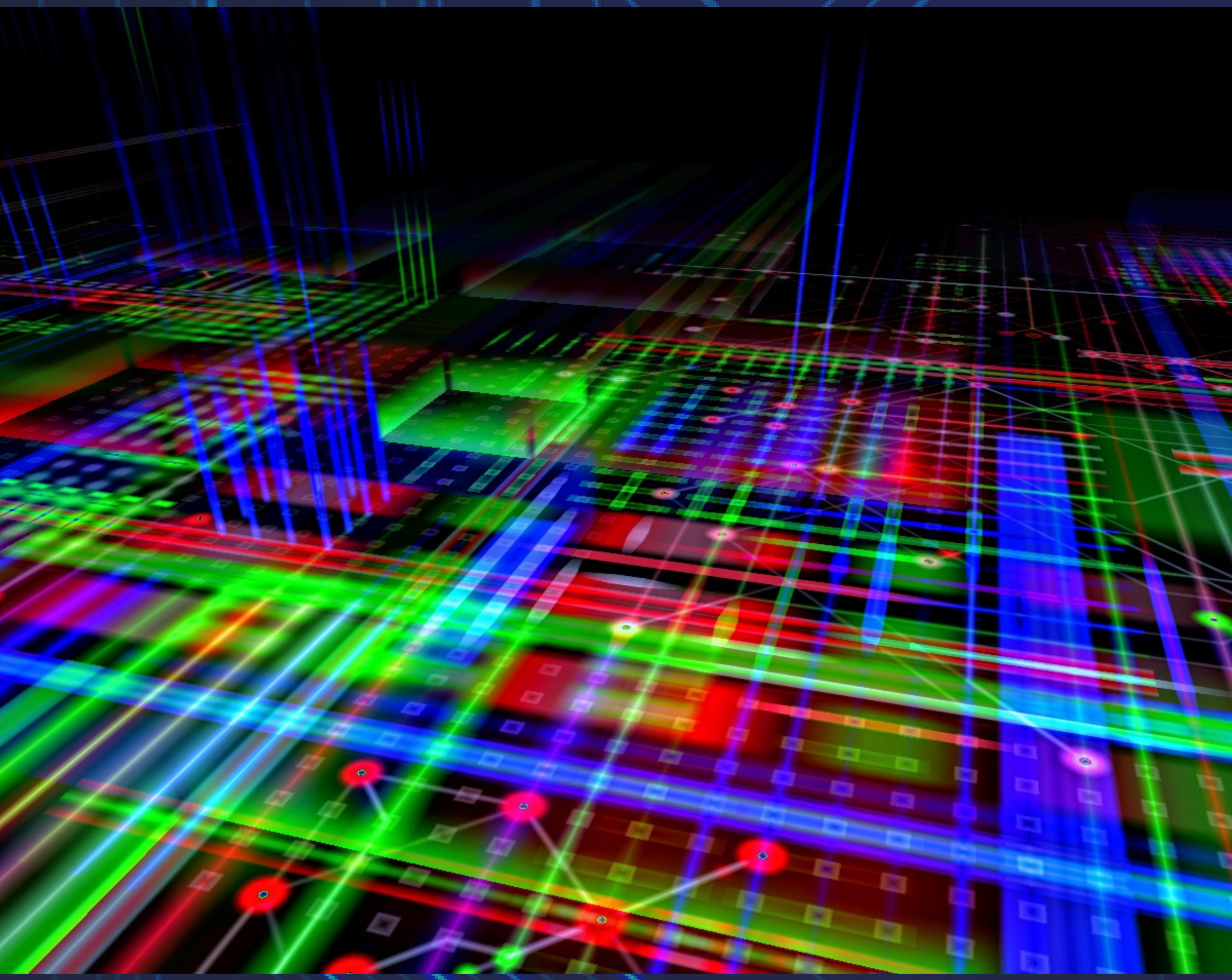
POLITEKNIK MALAYSIA

KEMENTERIAN PENGAJIAN TINGGI

KOLEJ KOMUNITI MALAYSIA

SCORE A+ DIGITAL ELECTRONICS

ELECTRICAL ENGINEERING DEPARTMENT



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This speech is also addressed to all parties who have been involved in the success of this task either directly or indirectly. All the help they have given is very much appreciated because without their help and support all these tasks may not be possible.

Thank you

How to learn fast??

How to solve this question???

I need example question...

Can I get what I need in one book?

What's in this e-book

Mind Maps

Example Questions & Answer

Synopsis

This e-book contains mind map for each chapter and previous final exam questions as a guide to students according to the topics studied.

Content

CHAPTER 1
NUMBER & CODE SYSTEM
PAGE 6-21

CHAPTER 2
BOOLEAN ALGEBRA
PAGE 22-40

CHAPTER 3
FLIP-FLOPS
PAGE 41-54

CHAPTER 4
COUNTERS
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REGISTERS
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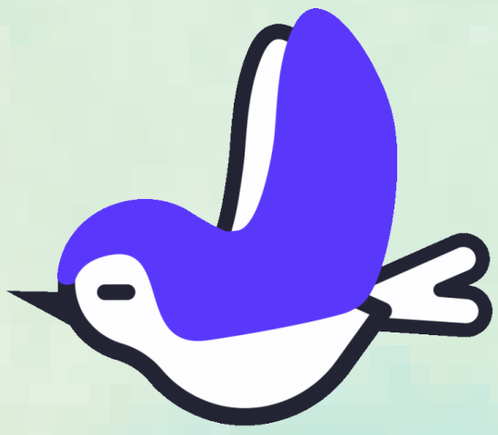
Chapter 1

Number & Code System



CONVERSION OF NUMBER SYSTEMS

TYPES OF NUMBER SYSTEMS

NUMBER SYSTEMS & CODE SYSTEMS

SIGNED NUMBERS

ASCII CODE

BCD CODE

GRAY CODE

Types Of Number Systems

BINARY

- Base 2
- Example : 11010_2

DECIMAL

- Base 10
- Example : 258_{10}

HEXADECIMAL

- Base 16
- Example : $12AC_{16}$

OCTAL

- Base 8
- Example : 125_8

CONVERSION OF NUMBER SYSTEMS

Octal → Decimal

$24.6_8 = (2 \times 8^1) + (4 \times 8^0) + (6 \times 8^{-1})$

$= 20.75_{10}$

Octal → Binary

$4\ 7\ 2_8 = \underbrace{1\ 0\ 0}_{4}\ \underbrace{1\ 1\ 1}_{7}\ \underbrace{0\ 1\ 0}_{2}{}_2$

Decimal → Octal

$\frac{266}{8} = 33.25 \longrightarrow 0.25 \times 8 = 2 \longrightarrow$ remainder of 2 (LSB)

$\frac{33}{8} = 4.125 \longrightarrow 0.125 \times 8 = 1 \longrightarrow$ remainder of 1

$\frac{4}{8} = 0.5 \longrightarrow 0.5 \times 8 = 4 \longrightarrow$ remainder of 4 (MSB)

$266_{10} = 4\ 1\ 2_8$

Binary → Octal

$1\ 0\ 1\ 1\ 1\ 0\ 1\ 0_2 = \underbrace{0\ 1\ 0}_{2}\ \underbrace{1\ 1\ 1}_{7}\ \underbrace{0\ 1\ 0}_{2}{}_8$

Decimal → Hexadecimal

Change 312.78_{10} into hexadecimal value

$\frac{312}{16} = 19 \longrightarrow$ remainder of 8 (LSB)

$\frac{19}{16} = 1 \longrightarrow$ remainder of 3

$\frac{1}{16} = 0 \longrightarrow$ remainder of 1 (MSB)

$0.78 \times 16 = 12.48$

$0.48 \times 16 = 7.68$

$0.68 \times 16 = 10.88$

$0.88 \times 16 = 14.08$

$156.78_{10} = 1\ 3\ 8\ .\ C7AE$

Hexadecimal → Decimal

$3\ 5\ 6_{16} = (3 \times 16^2) + (5 \times 16^1) + (6 \times 16^0)$

$= 854_{10}$

Conversion of Number Systems

Hexadecimal ➡ Binary

$ABF.2_{16} = \underbrace{1010}_{A}\ \underbrace{1011}_{B}\ \underbrace{1111}_{F}.\ \underbrace{0010}_{2}{}_2$

Binary ➡ Hexadecimal

$101110100110_2 = \underbrace{1011}_{B}\ \underbrace{1010}_{A}\ \underbrace{0110}_{6}$

$= BA6_{16}$

Binary ➡ Decimal

$1101.11_2 = (1x2^3) + (1x2^2) + (0x2^1) + (1x2^0) + (1x2^{-1}) + (1x2^{-2})$

$= 8 + 4 + 1 + 0.5 + 0.25$

$= 13.75_{10}$

Decimal ➡ Binary

37_{10} ➡ Binary number

37 / 2	= 18.5	⟶	remainder of 1 (LSB)
18 / 2	= 9.0	⟶	remainder of 0
9 / 2	= 4.5	⟶	remainder of 1
4 / 2	= 2.0	⟶	remainder of 0
2 / 2	= 1.0	⟶	remainder of 0
1 / 2	= 0.5	⟶	remainder of 1 (MSB)

$37_{10} = 100101_2$

ADDITION & SUBSTRACTION OF NUMBER SYSTEMS

+ of Binary

```
  1 0 1 0
+ 1 1 1 1
---------
1 1 0 0 1
---------
```

- of Binary

```
  1 0 1 0
- 0 1 1 1
---------
  0 0 1 1
---------
```

+ of Octal

```
  5 6 4 8
+ 7 7 7 8
---------
1 5 6 3 8
---------
```

- of Octal

```
  6 2 1 8
- 2 6 7 8
---------
  3 3 2 8
---------
```

+ of Hexadecimal

```
    A B C
+   7 7 7
---------
1 2 3 3
---------
```

- of Hexadecimal

```
    6 2 1 16
-   2 6 7 16
-------------
    3 B A 16
-------------
```

SIGNED NUMBERS

1's Complement

- Negative Binary Numbers : 1's complement is the reversal of that binary numbers.
- Positive Binary Numbers : 1's complement is the same as the binary numbers.

2's Complement

- Negative Binary Numbers : 2's complement is the reversal of binary number and added up with 1.
- Positive Binary Numbers :2's complement is the same as binary numbers.

Example 1

$-12_{10} + (14_{10}) = 2_{10}$

DECIMAL	BINARY	1'S COMPLEMENT	2'S COMPLEMENT	OPERATION
-12	00001100	11110011	11110011 + 1 11110100	11110100 +00001110 ----------
+14	00001110	00001110	00001110	100000010

Example 2

$+12_{10} + (-14_{10}) = -2_{10}$

DECIMAL	BINARY	1'S COMPLEMENT	2'S COMPLEMENT	OPERATION
+12	00001100	00001100	00001100	00001100
-14	00001110	11110001	11110001 + 1 ---------- 11110010	+11110010 ---------- 11111110

ASCII Code

Definition

American Standard Code for Information Interchange

Example

This message 48 45 4C 50 has been coded in ASCII codes. What is the meaning of the messages?

Answer : HELP

Table of ASCII Codes

MSB / LSB	Binary	000	001	010	011	100	101	110	111
Binary	Hex	0	1	2	3	4	5	6	7
0000	0	Nul	Del	sp	0	@	P		p
0001	1	Soh	Dc1	!	1	A	Q	a	q
0010	2	Stx	Dc2	"	2	B	R	b	r
0011	3	Etx	Dc3	#	3	C	S	c	s
0100	4	Eot	Dc4	$	4	D	T	d	t
0101	5	End	Nak	%	5	E	U	e	u
0110	6	Ack	Syn	&	6	F	V	f	v
0111	7	Bel	Etb	'	7	G	W	g	w
1000	8	Bs	Can	(	8	H	X	h	x
1001	9	HT	Em	)	9	I	Y	i	y
1010	A	LF	Sub	.	:	J	Z	j	z
1011	B	VT	Esc	+	;	K		k	
1100	C	FF	FS	,	<	L		l	
1101	D	CR	GS	-	=	M		m	
1110	E	SO	RS	.	>	N		n	
1111	F	SI	US	/	?	O		o	

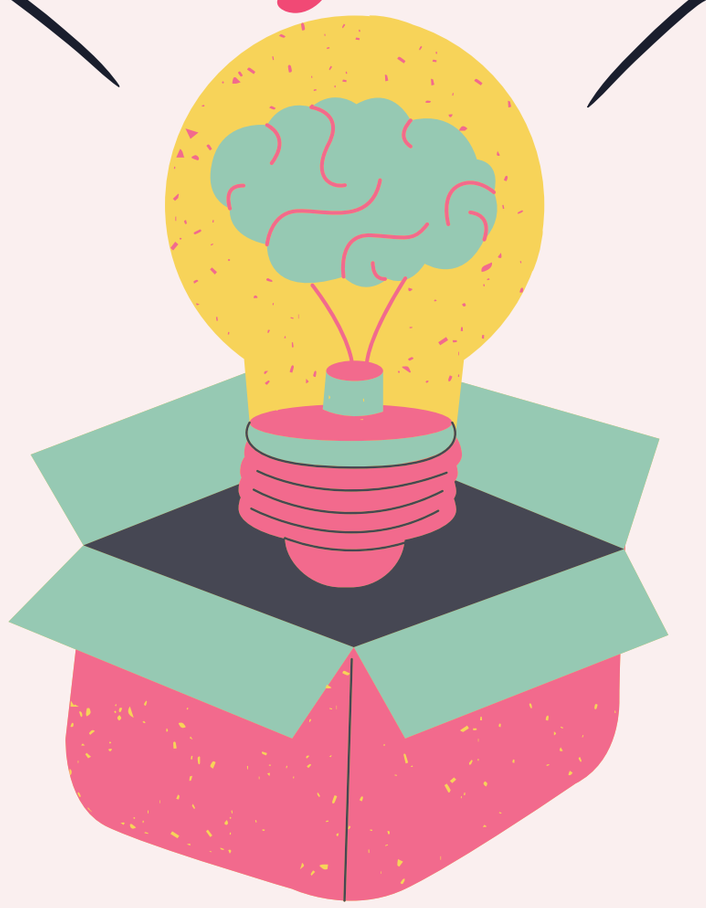
Definition

A gray code represents numbers using a binary encoding scheme that groups a sequence of bits so that only one bit in the group changes from the number, before and after.

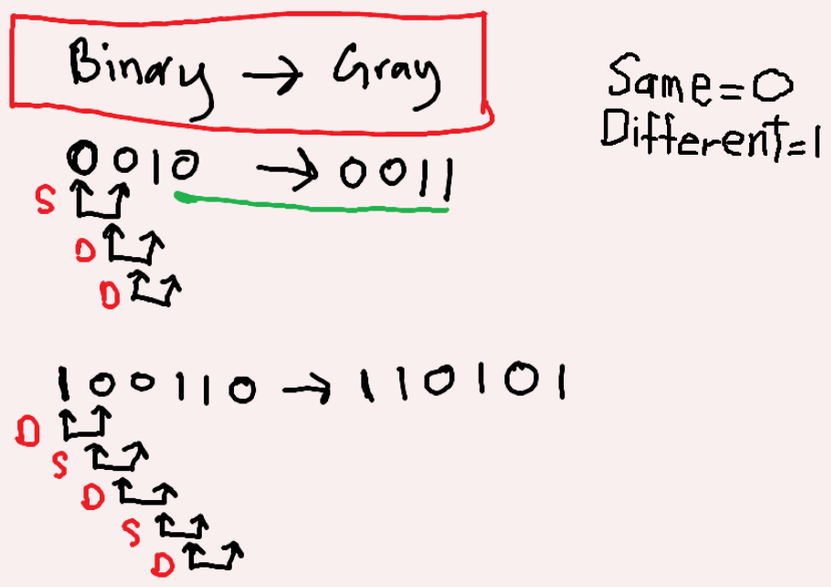
Gray code table

Decimal	Binary	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111

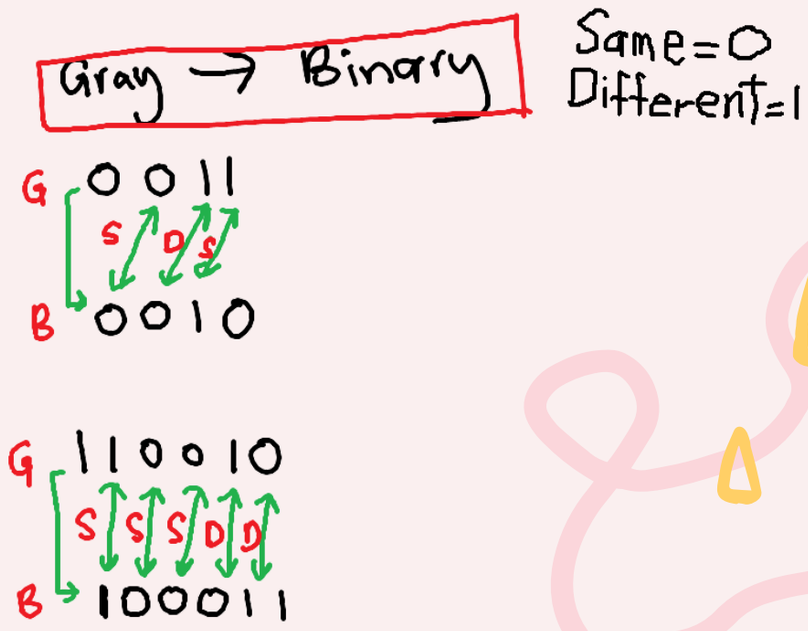
Gray Code



Binary → Gray Code



Gray Code → Binary



Question 1

a) State the BCD 8421 code for 827_{10}

b) By applying the correct method, convert the following numbers $A56.BD_{16}$ and 0111 0011 0001(BCD) to octal number systems.

c) Complete the 8 bits arithmetic operation of this decimal number in 2's complement.

$$45_{10} + (-37_{10}) =$$

Question 2

a) State 127_8 in binary number.

b) Convert the BCD code 10000111 to its equivalent binary and hexadecimal number.

c) Solve the 8 bits arithmetic operation below using 2's complement method.

$$(-13)_8 + 22_{10} =$$

Question 3

a) State 216_8 in hexadecimal equivalent.

$$87_{10} - 62_{10} =$$

b) Solve the 8 bits arithmetic operation below using 2's complement method.

c) Convert the numbers below to BCD 8421 codes.

i. 45_{10}

ii. 637_8

Question 4

a) State 110010_2 in decimal number.

b) Convert the BCD code 10000100011 to its equivalent binary & octal number.

c) Illustrate the 8 bit addition of this decimal number in 2's complement.

$$(-13_{10}) + (+20_{10}) =$$

Question 5

a) Write the binary & hexadecimal numbers in Table 1.

Decimal	Binary	Hexadecimal
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		

Table 1

b) Convert 11000011110.11_2 to decimal, octal and hexadecimal numbers.

c) Complete the 8 bits addition of decimal number below in 2's complement representation.

$$(-57)_{10} + (-38)_{10} =$$

Question 6

a) State 567_8 in binary equivalent.

b) Convert the following BCD codes to binary numbers 00111000 (BCD) and 01001001 (BCD).

c) Solve the 8 bits arithmetic operation below by using 2's complement method.

$$(+16)_{10} + (-24)_{10} =$$

Question 7

a) State $8E76_{16}$ in binary number.

b) Convert 10001010101.101_2 to decimal, octal and hexadecimal numbers.

c) Solve the 8 bits addition of decimal number below using 2's complement.

$$(-42)_{10} + (-35)_{10} =$$

Question 8

a) Change the BCD code 100101111000 to its equivalent binary and octal.

b) Solve the 8 bits addition of decimal number below using 2's complement.

$$(-26)_{10} + (+18)_{10} =$$

ANSWERS

Q.1.a) 100000100111

Q.1.b) i) $A56.BD_{16} = 5126.57_8$

Q.1.b.ii) 1333_8

Q.1.c) 1000010000_2

Q.2.a) 001010111_2

Q.2.b.i) 1010111_2

Q.2.b.ii) 57_{16}

Q.2.c) 100001001_2

Q.3.a) $8E_{16}$

Q.3.b) 00011001_2

Q.3.c.i) 01000101

Q.3c.ii) 010000010101

Q.4.a) 50_{10}

Q.4.b) binary : 110100111_2

octal : 647_8

Q.4.c) 00000111_2

Q.5.a)

DECIMAL	BINARY	HEXADECIMAL
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Q.5.b) Decimal : 1566.75_{10}

Octal : 3036.6_{8}

Hexadecimal : $61C.C_{16}$

Q.5.c) 110100001_{2}

Q.6.a) 101110111_2

Q.6.b.i) 100110_2

Q.6.b.ii) 110001_2

Q.6.c) 10000100_2

Q.7.a) 1000111001111111_2

Q.7.b) Decimal : 1109.625_{10}

Octal : 2125.5_8

Hexadecimal : $455.A_{16}$

Q.7.c) 110110011_2

Q.8.a) Binary : $111101001 0_2$

Octal : 1722_8

Q.8.b) 11010100_2

Chapter 2
Boolean Algebra

Boolean Operation

Basic Gates

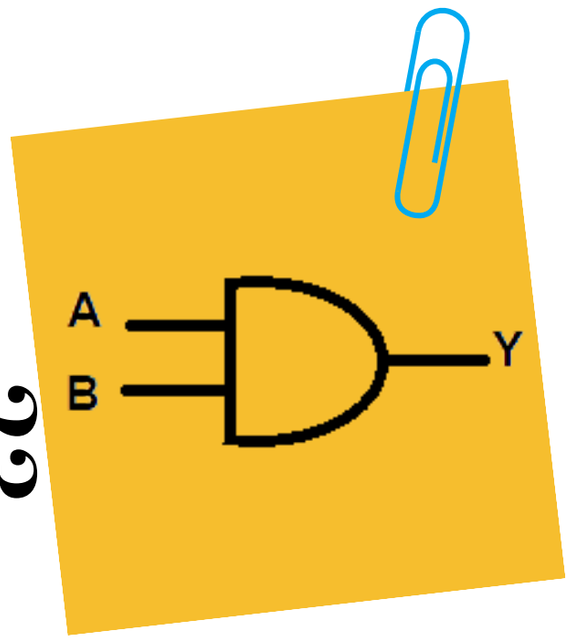
Methods To Simplify Boolean Equation

Logic Gates Replacement

Combinational Logic Circuit

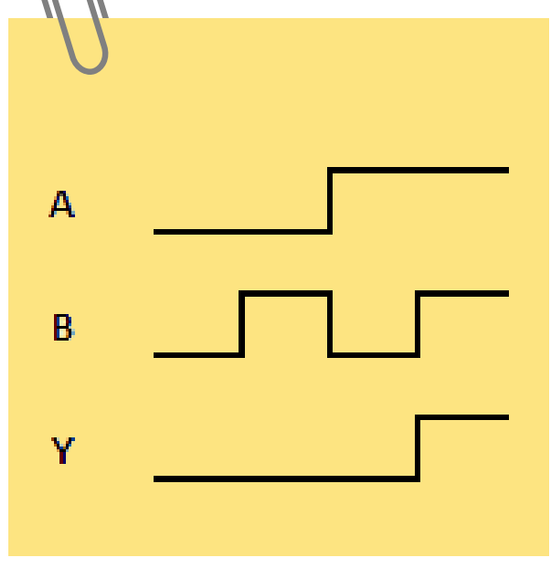
BASIC GATES

AND Gate

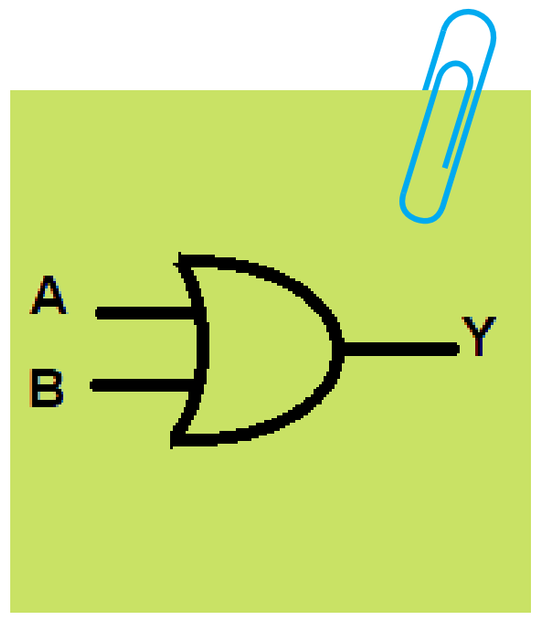


$$Y = A.B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

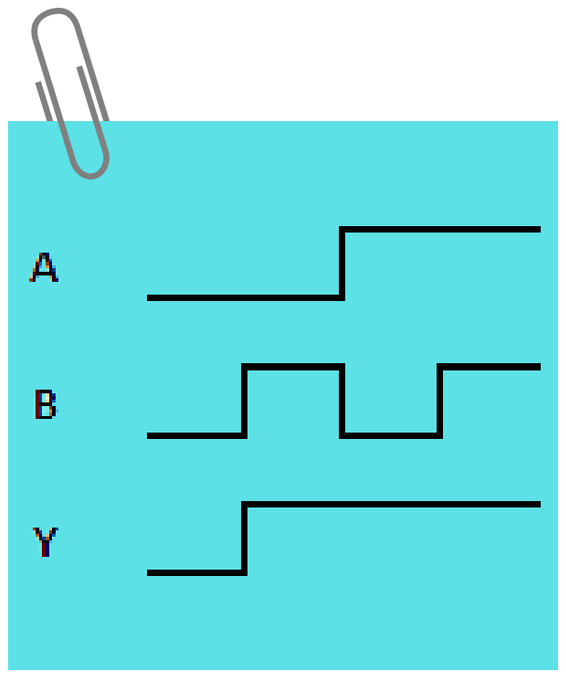


OR Gate

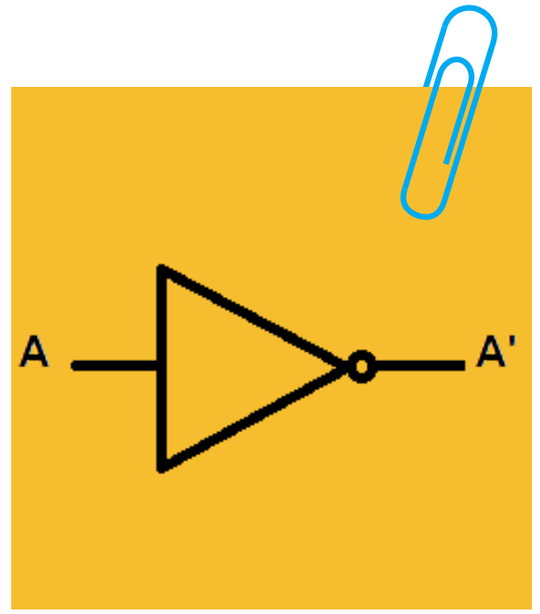


$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

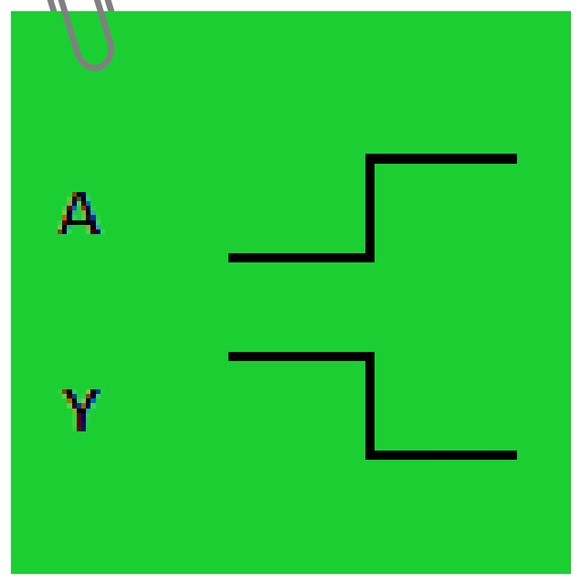


NOT Gate



$$Y = A'$$

A	Y
0	1
1	0

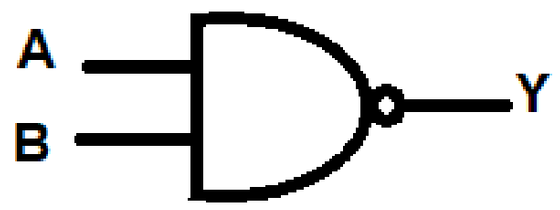


Mastering basic gates using this mind map

BASIC GATES

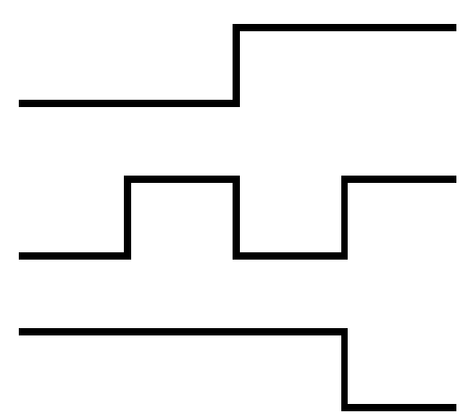
Remember the symbol, function & the boolean equation

NAND GATE

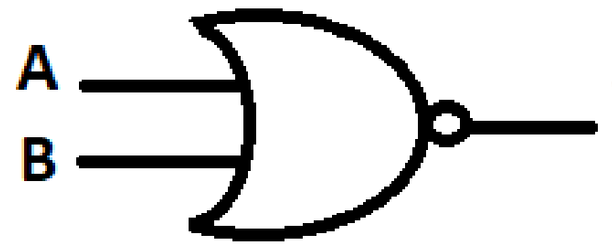


$Y = (A+B)'$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

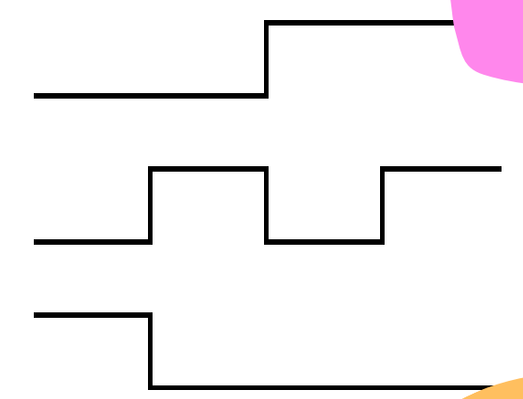


NOR GATE



$Y = (A+B)'$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

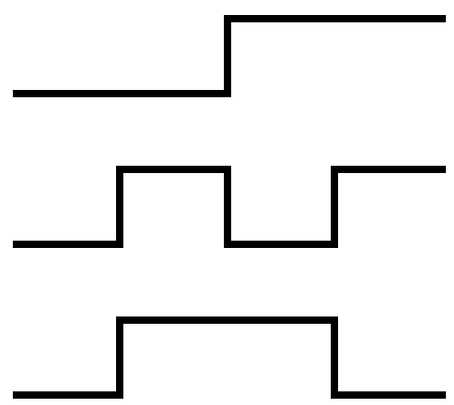


Basic gates are the heart of digital systems

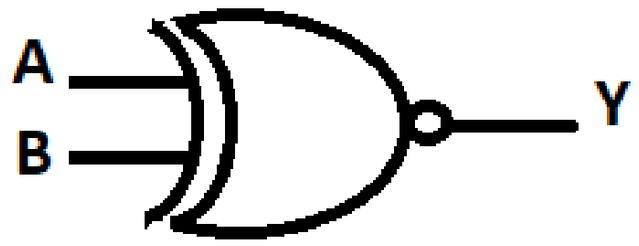
EX-OR GATE

$Y = A \oplus B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

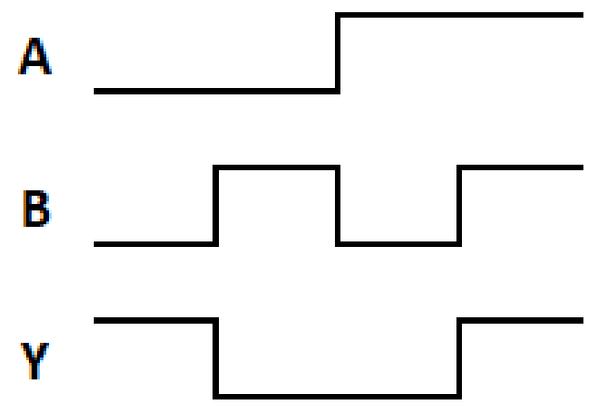


EX-NOR GATE



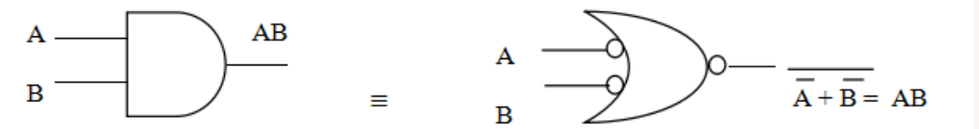
$Y = (A \oplus B)'$

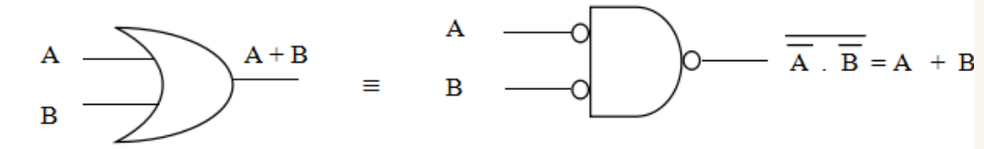
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



LOGIC GATES REPLACEMENT

Standard Symbols

1)


2)


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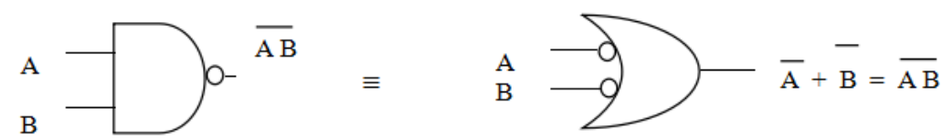

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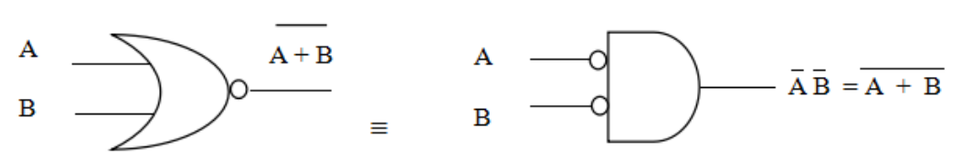

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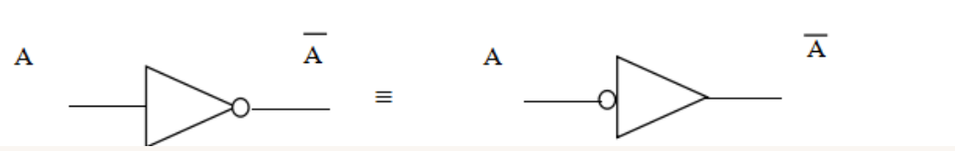
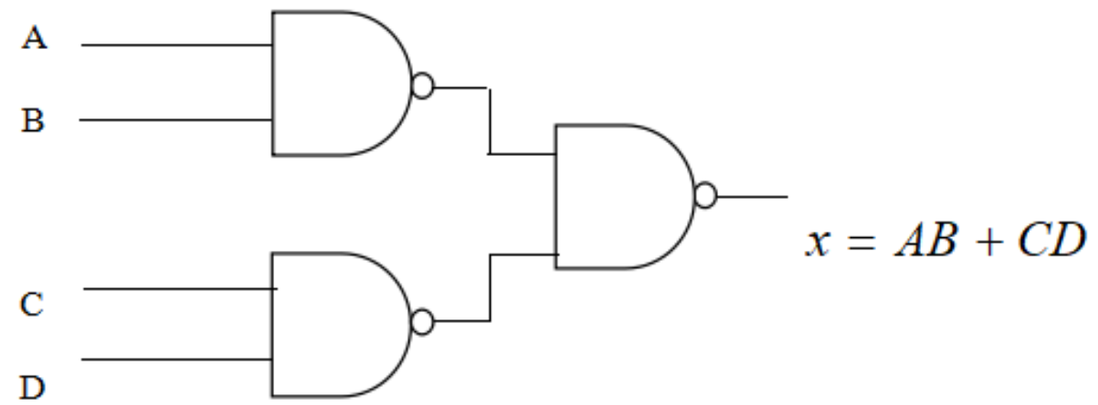
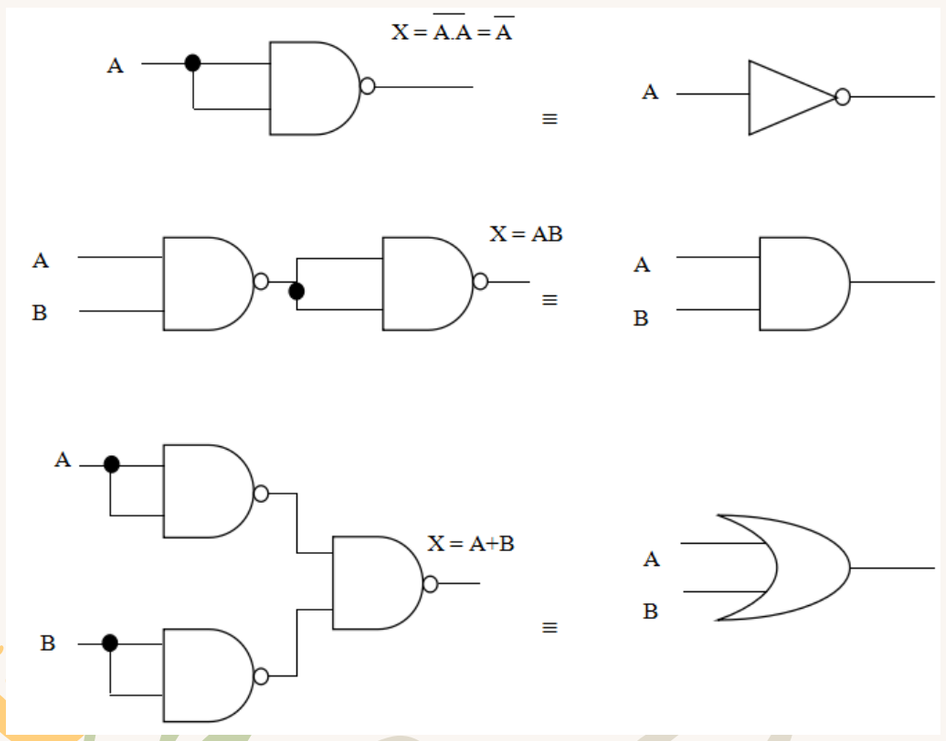


Example

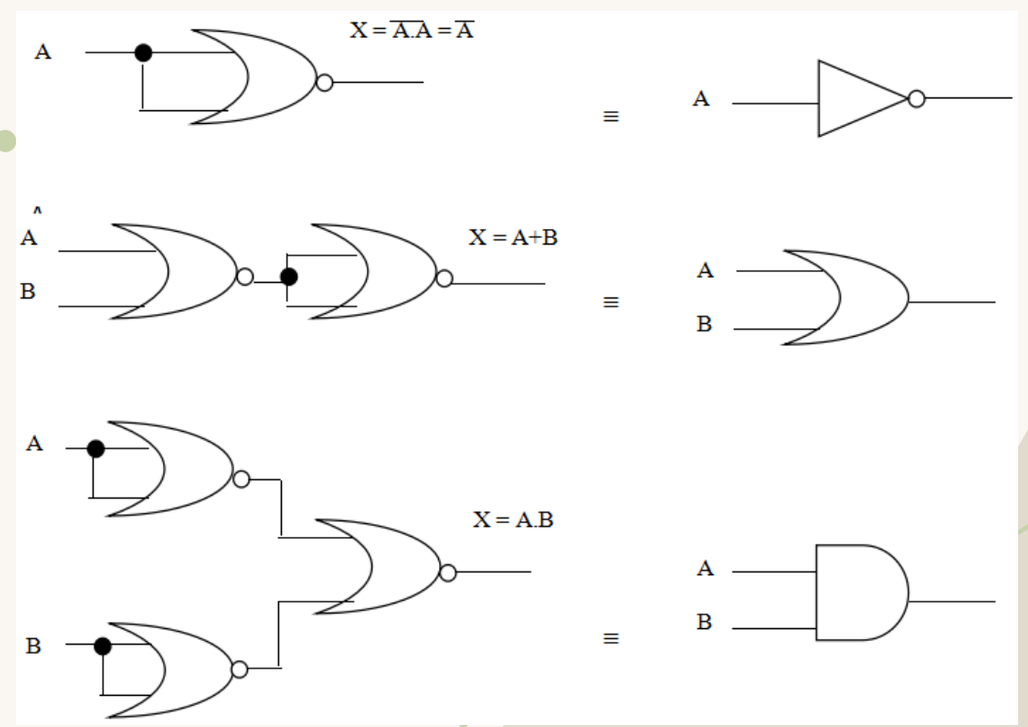
Implement a logic circuit having the output expression $x = AB + CD$ using NAND gate only.



Usage For NAND Gate



Usage For NOR Gate



COMBINATIONAL LOGIC CIRCUIT

DEFINITION

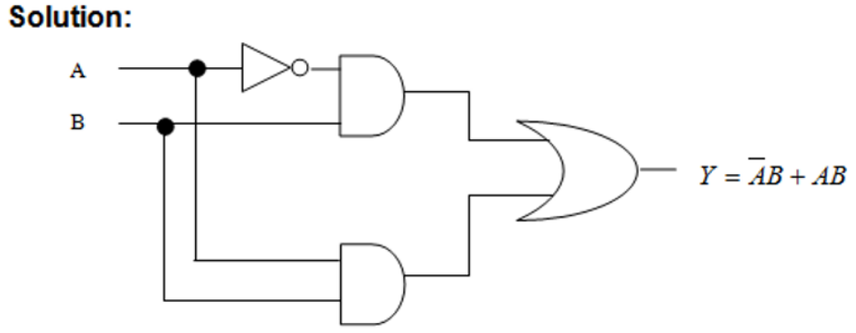
Combinational logic circuit means combination of basic gates in one circuit.

EXAMPLE 1

Let's examine the expression:

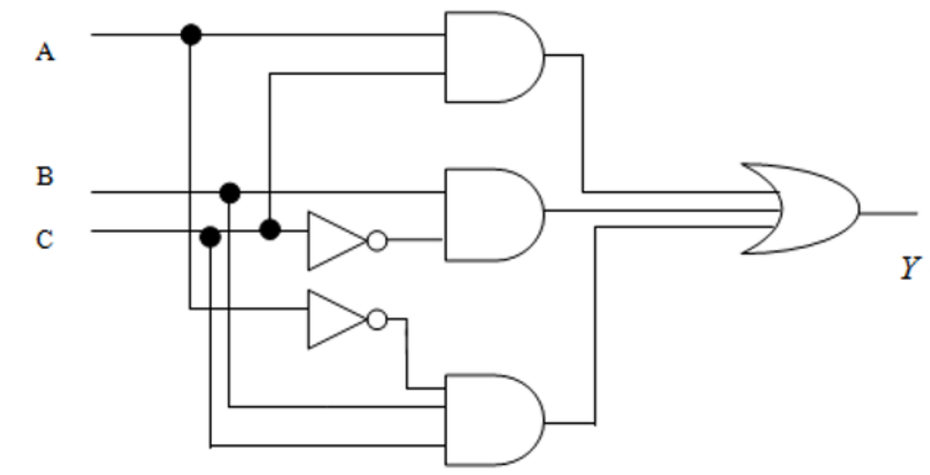
$Y = \overline{A}B + AB$

Solution:



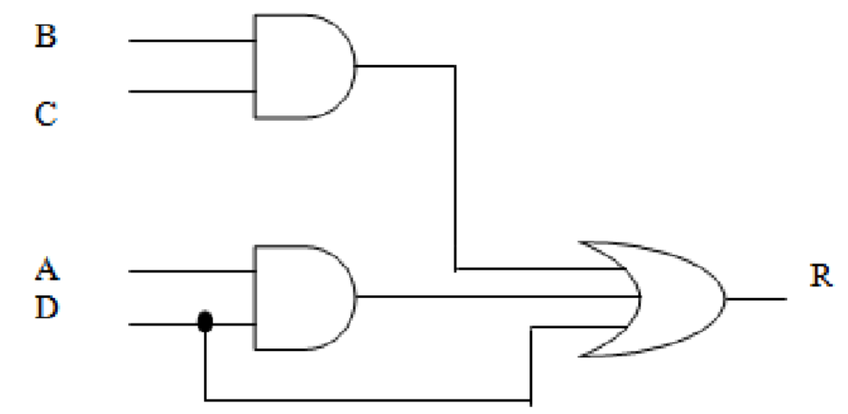
EXAMPLE 2

Given logic equation: $Y = AC + B\overline{C} + \overline{A}BC$



EXAMPLE 3

Derive the Boolean equation for the logic circuit below.



$R = BC + AD + D$

METHODS TO SIMPLIFY BOOLEAN EQUATION

BOOLEAN LAW

KARNAUGH MAP (K-MAP)

BOOLEAN LAWS

AND LAW

$X.0 = 0$

$X.1 = X$

$X.X = X$

$X.\overline{X} = 0$

OR LAW

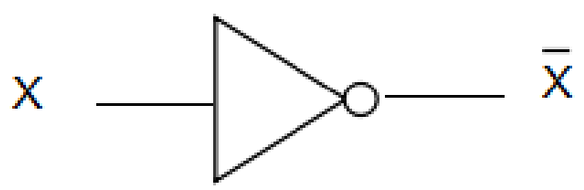
$X + 0 = X$

$X + 1 = 1$

$X + X = X$

$X + \overline{X} = 1$

NOT LAW



COMMUTATIVE LAW

$X + Y = Y + X$

$X.Y = Y.X$

BOOLEAN LAWS

Absorption Law

$$X + XY = X$$
$$X(X + Y) = X$$
$$\overline{X} + XY = \overline{X} + Y$$
$$X + \overline{X}Y = X + Y$$
$$X(X + \overline{Y}) = XY$$

De Morgan Theorem

$$\overline{X + Y} = \overline{X}.\overline{Y}$$
$$\overline{X.Y} = \overline{X} + \overline{Y}$$

Distribution Law

$$X(Y + Z) = XY + XZ$$
$$(W + X)(Y + Z) = WY + XY + WZ + XZ$$

Associative Law

$$X(YZ) = (XY)Z = XYZ$$
$$X + (Y + Z) = (X + Y) + Z = X + Y + Z$$

KARNAUGH MAP

2 VARIABLES

Y = A'B'+AB

A \ B	0	1
0	1	0
1	0	1

Group 1

Y = A'

A \ B	0	1
0	1	1
1	0	0

Group 2

Y = 1

A \ B	0	1
0	1	1
1	1	1

Group 4

3 VARIABLES

Y = B'C'

AB \ C	0	1
00	1	0
01	0	0
11	0	0
10	1	0

Group 2

Y = B'

AB \ C	0	1
00	1	1
01	0	0
11	0	0
10	1	1

Group 4

Y = 1

AB \ C	0	1
00	1	1
01	1	1
11	1	1
10	1	1

Group 8

Y = A'B'C' + AB'C

AB \ C	0	1
00	1	0
01	0	0
11	0	0
10	0	1

Group 1

4 VARIABLES (K-MAP)

Group 1

Y = A'B'CD + A'BC'D + AB'CD'

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	0	0	0	0
10	0	0	1	0

Group 2

Y = A'B'C' +ABC

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	0	0	1	1
10	0	0	0	0

Group 4

Y = A'C'

AB \ CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

Group 8

Y = A'

AB \ CD	00	01	10	11
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

Group 16

Y = 1

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

Question 1

a) State the logic gate type and truth table for the logic gate in Figure 1 below.

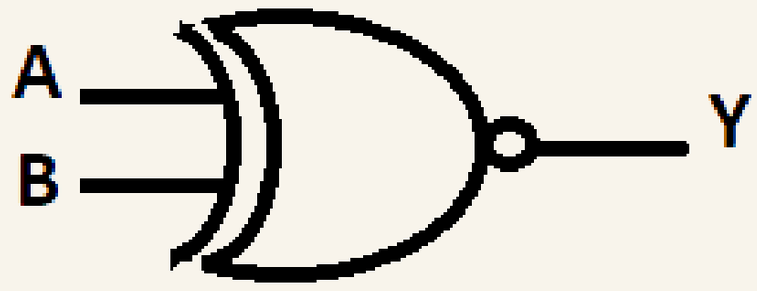


Figure 1

b) Represent the expression below with the suitable logic circuit.

$$X = ABC + A'BC + AB'C + A'B'C'$$

c) Given F (A,B,C,D)$=\sum(3, 10, 11, 13, 14, 15)$. Construct a truth table and simplify SOP equation using K=Map.

Question 2

a) Given a logic circuit as in Figure 2 below.

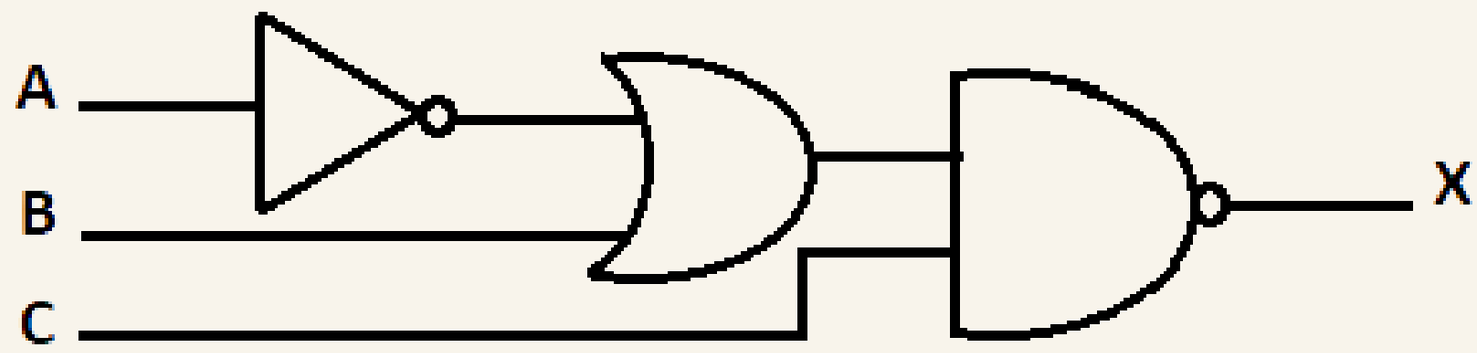


Figure 2

b) Apply Algebra Boolean Law to simplify the equation X = [(A + B')](B + C)]B .

c) Using K-Map , derive a simplified equation for :

X = BC'D' + A'BC'D + A'BCD + ABCD

Question 3

a) Draw the symbol of 2 input EX-OR gate, where A and B are the inputs and Y is the output. State the logic expression.

b) Based on the truth table in Table 1, produce the boolean equation in SOP form and simplify the equation using algebra Boolean Law.

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 1

Question 4

a) A 4 bits binary number is represented as A, B, C, D where D is the LSB. These binary numbers are the input to a logic circuit that will produce a HIGH output whenever the binary number id greater than 0011 and lesser than 1100. from the respective logic circuit design, get the truth table for the design problem above. By using K-Map, get the simplest boolean equation and draw the logic circuit from the simplified equation.

Question 5

a) Identify the logic gate for the boolean equation below.

$$Y = A'B$$

b) Simplify the following equation using K-Map.

$$Y = C(A'B' + B) + ABC' + AB$$

Question 6

Construct the truth table and simplify the equation using K-Map. Then draw the logic circuit based on the simplified equation.

Y = A'B'C'D + A'B'CD + A'BC'D' + A'BCD' + AB'C'D + AB'CD

Question 7

a) Refer Figure 3, write the truth table for this logic gate.

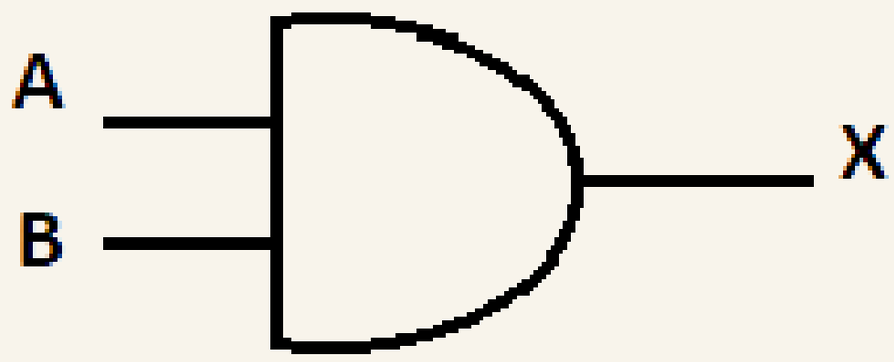


Figure 3

b) Simplify the following boolean equation using K-Map.

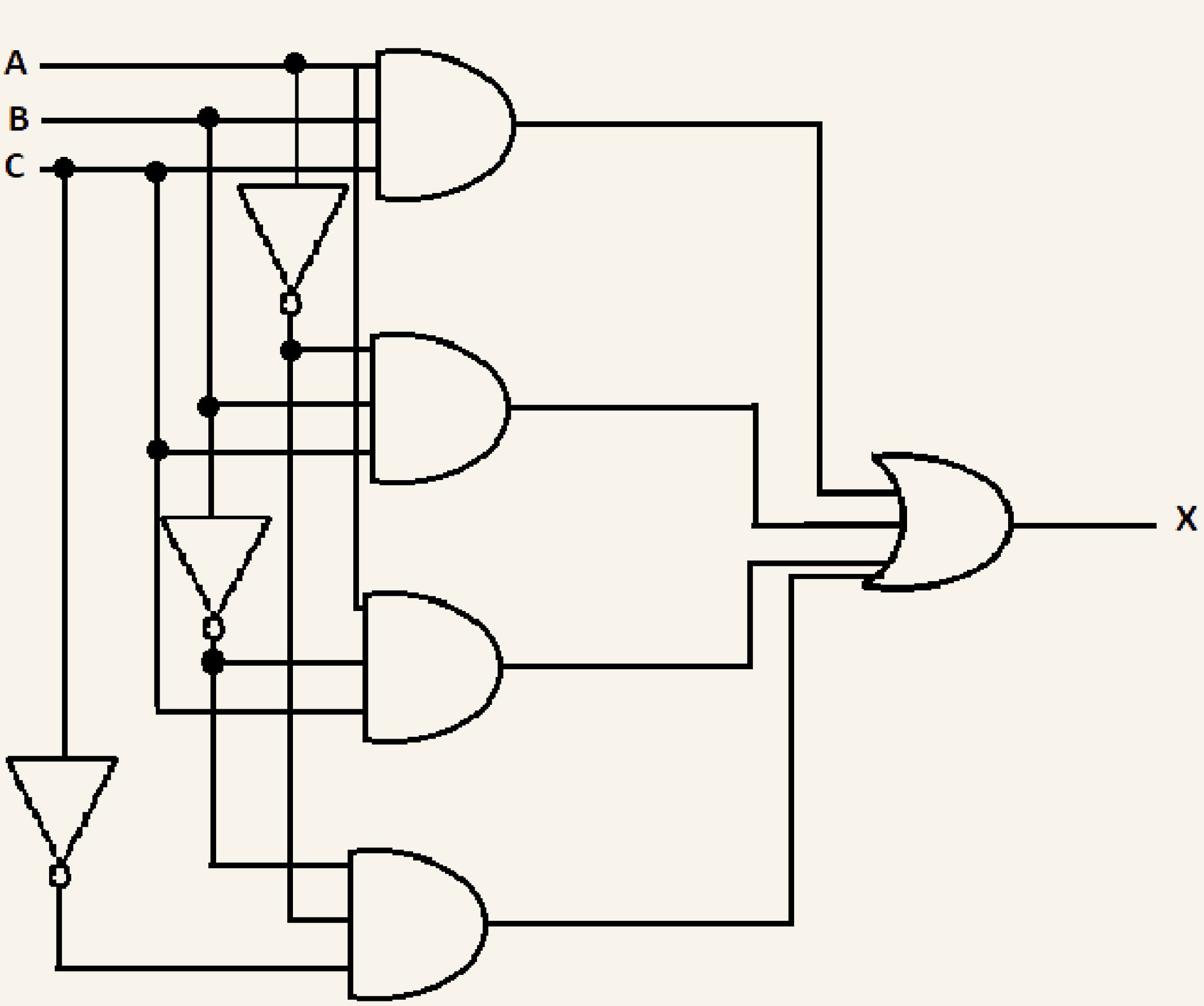
Z = A'B'C' + A'BC + A'BC' + ABC' + ABC + AB'C

ANSWERS :

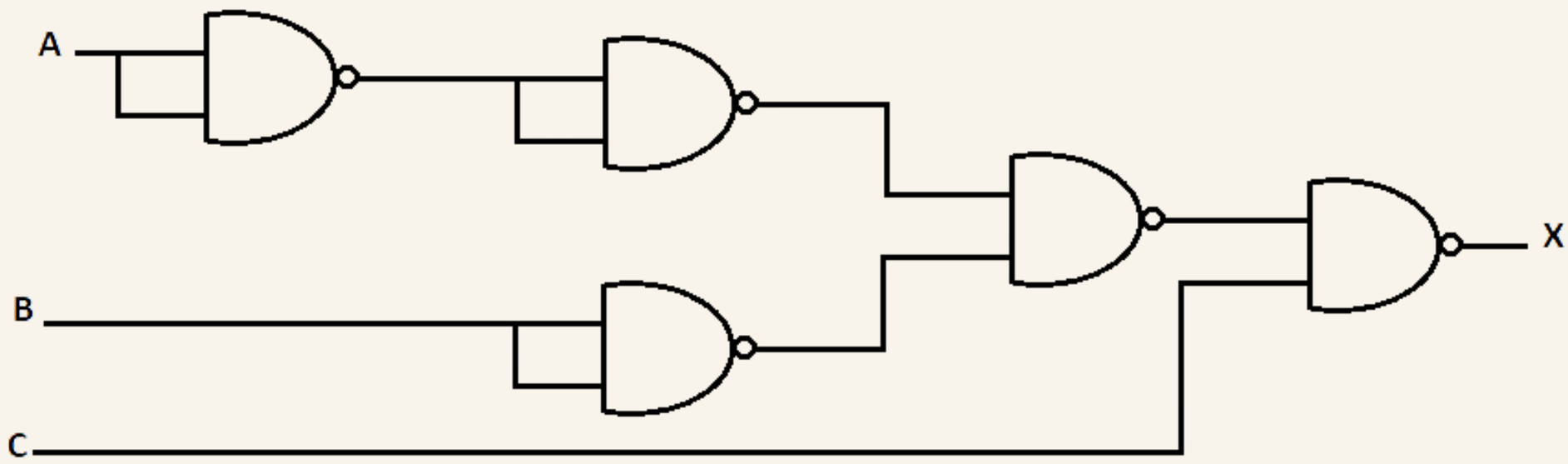
Q.1.a) EX-NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Q.1.b)



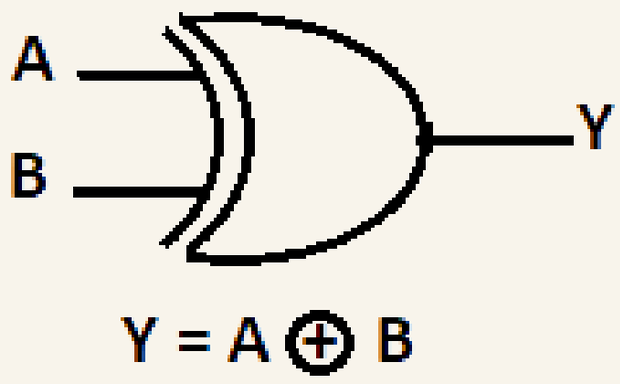
Q.2.a) X = [(A' + B)C]'



Q.2.b) X = AB

Q.2.C) X= BC' + BD

Q.3.a)



Q.3.b) Y = A'B' + B'C' + BC

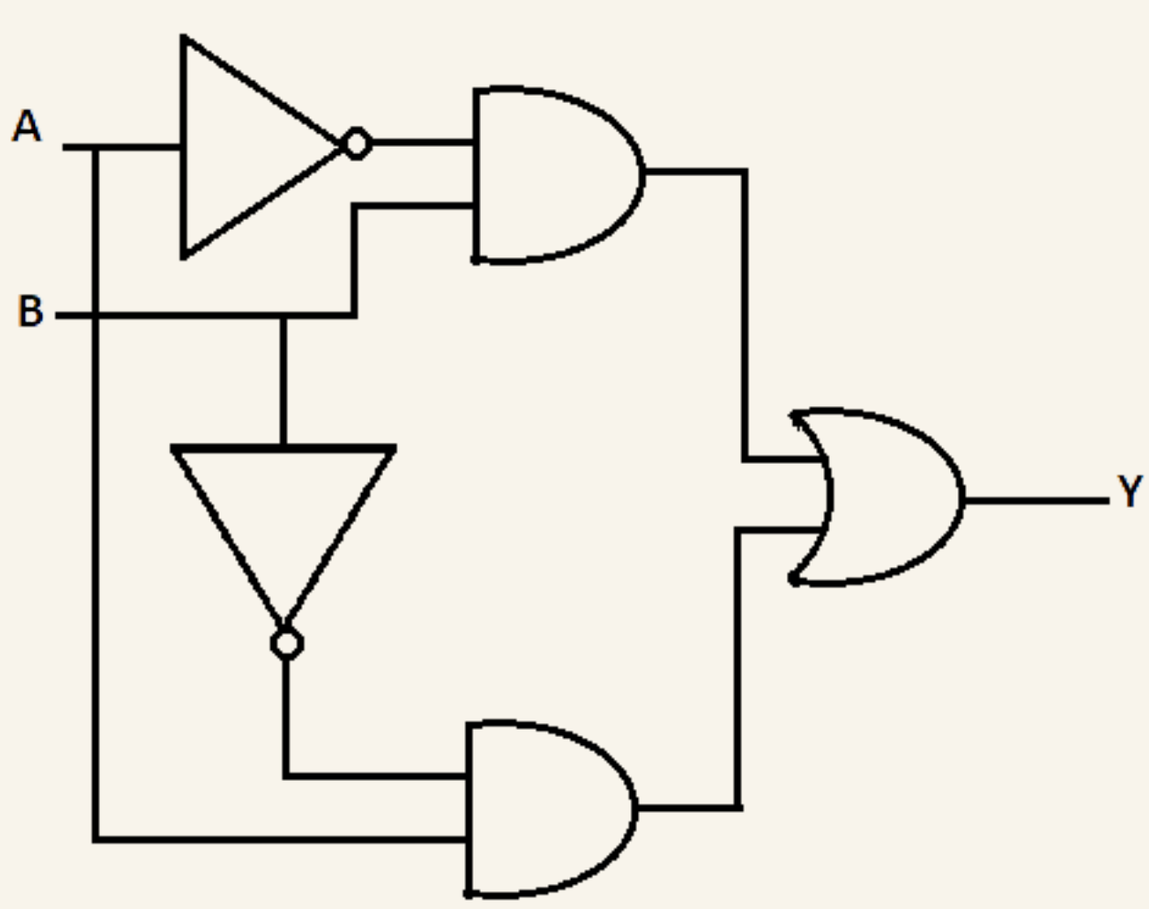
Q.4)

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Simplified equation :

Y = A'B + AB'

Simplified logic circuit :



Q.5.a)

- NOT gate
- AND gate

Q.5.b) Y = AB + A'C

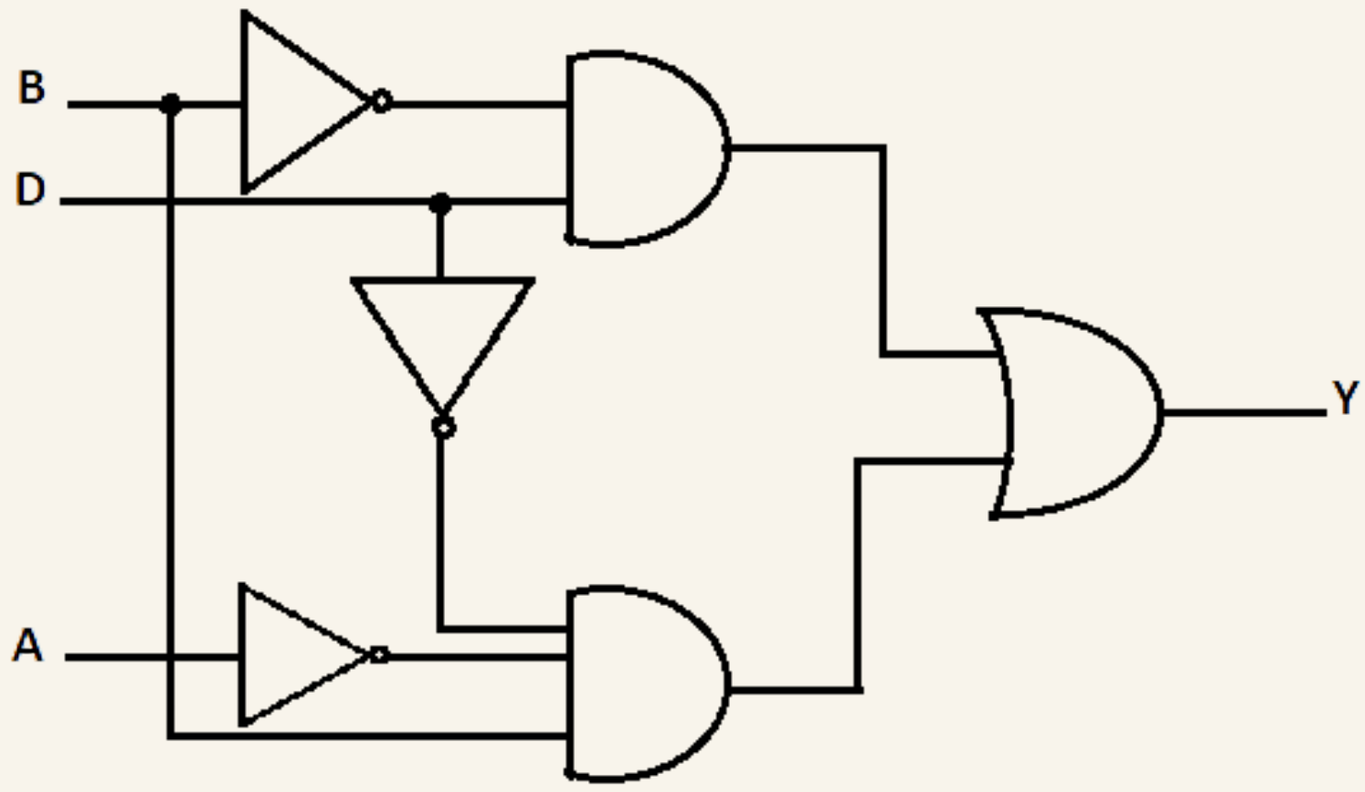
Q.6)

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Simplified equation :

Y = B'D + A'BD'

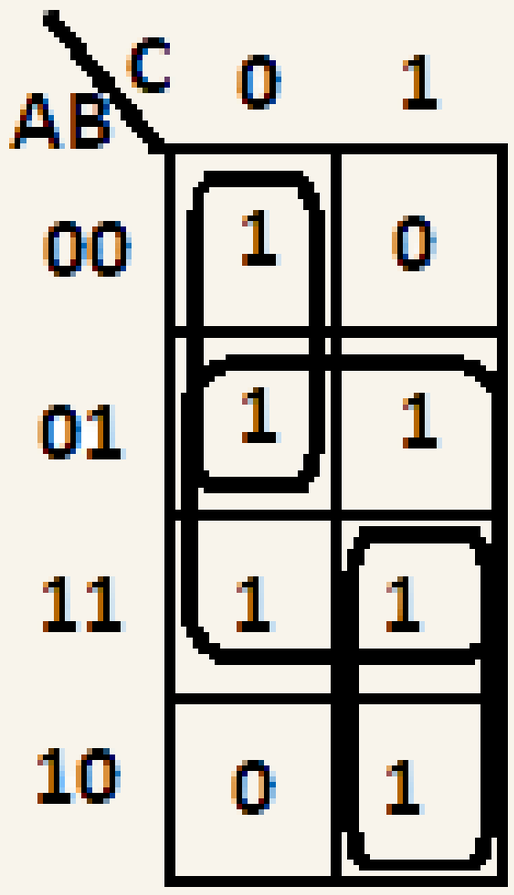
Logic circuit :



Q.7.a)

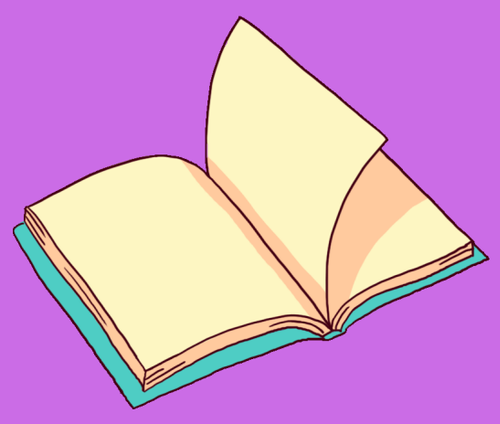
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Q.7.b)



Z = B + A'C' + AC

Chapter 3
Flip-Flops



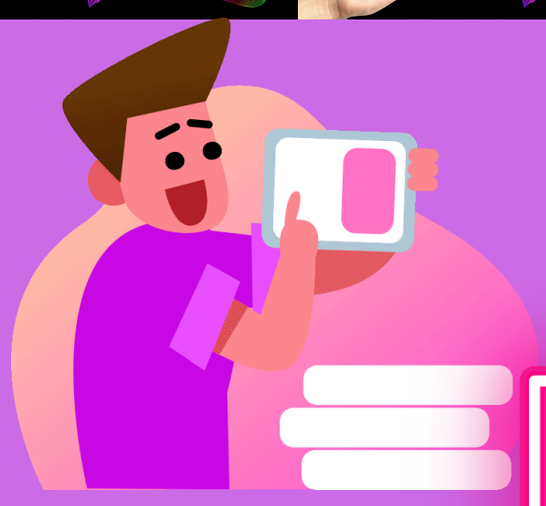
FLIP FLOP

UNCLOCKED FLIP FLOP

- NOR SR FLIP FLOP
- NAND SR FLIP FLOP

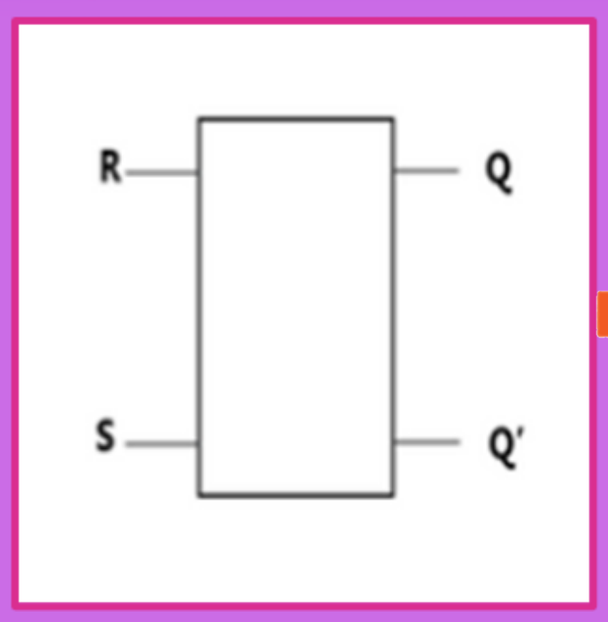
CLOCKED FLIP FLOP

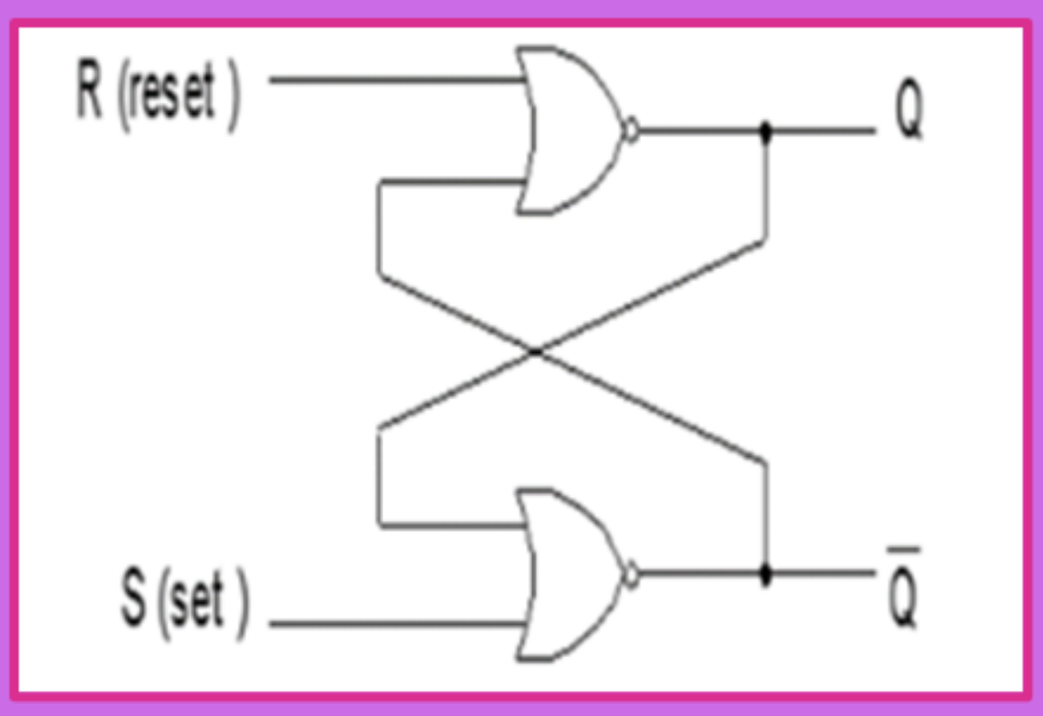
- SR FLIP FLOP
- JK FLIP FLOP
- T FLIP FLOP
- D FLOP FLOP



UNCLOCKED FLIP FLOP

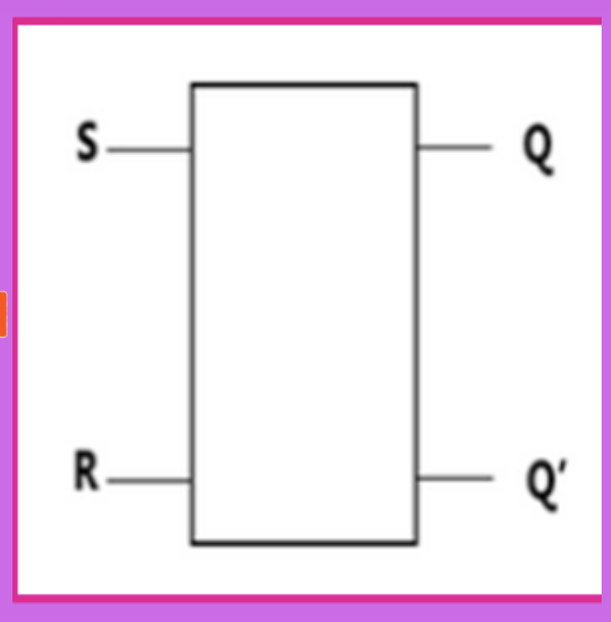
NOR SR FLIP FLOP

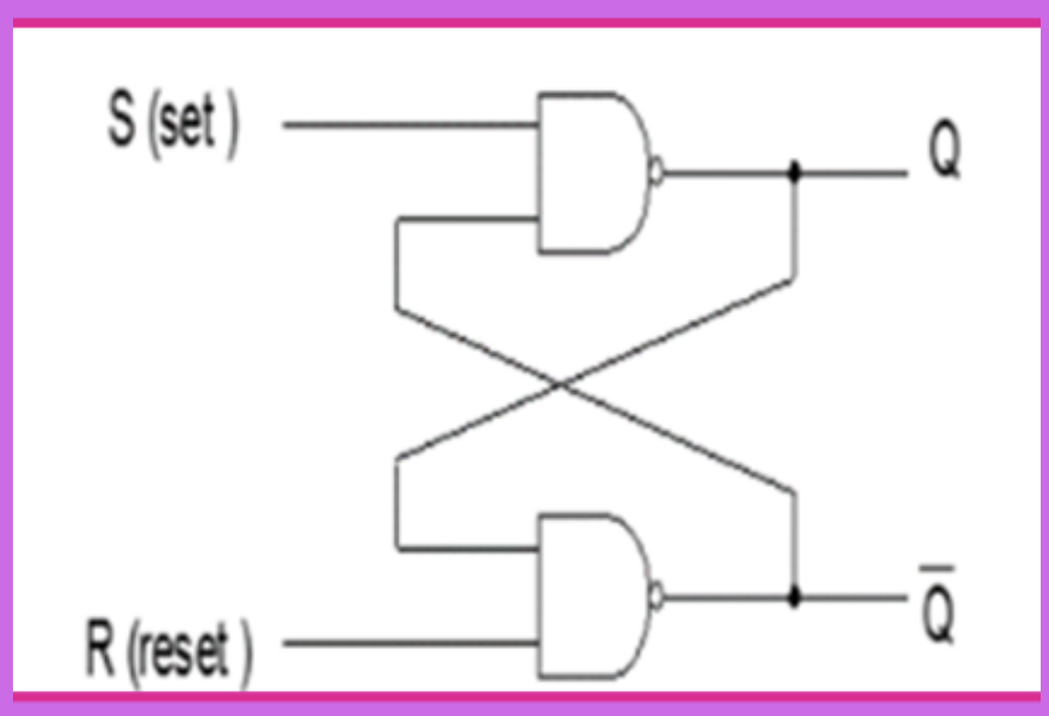




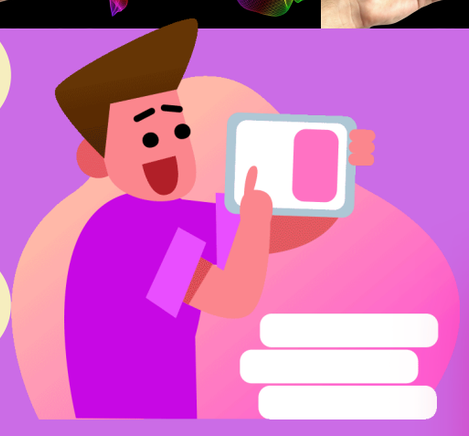
S	R	Q	$\bar{Q}$	OPERATION
0	0	0	1	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	1	1	Invalid

NAND SR FLIP FLOP





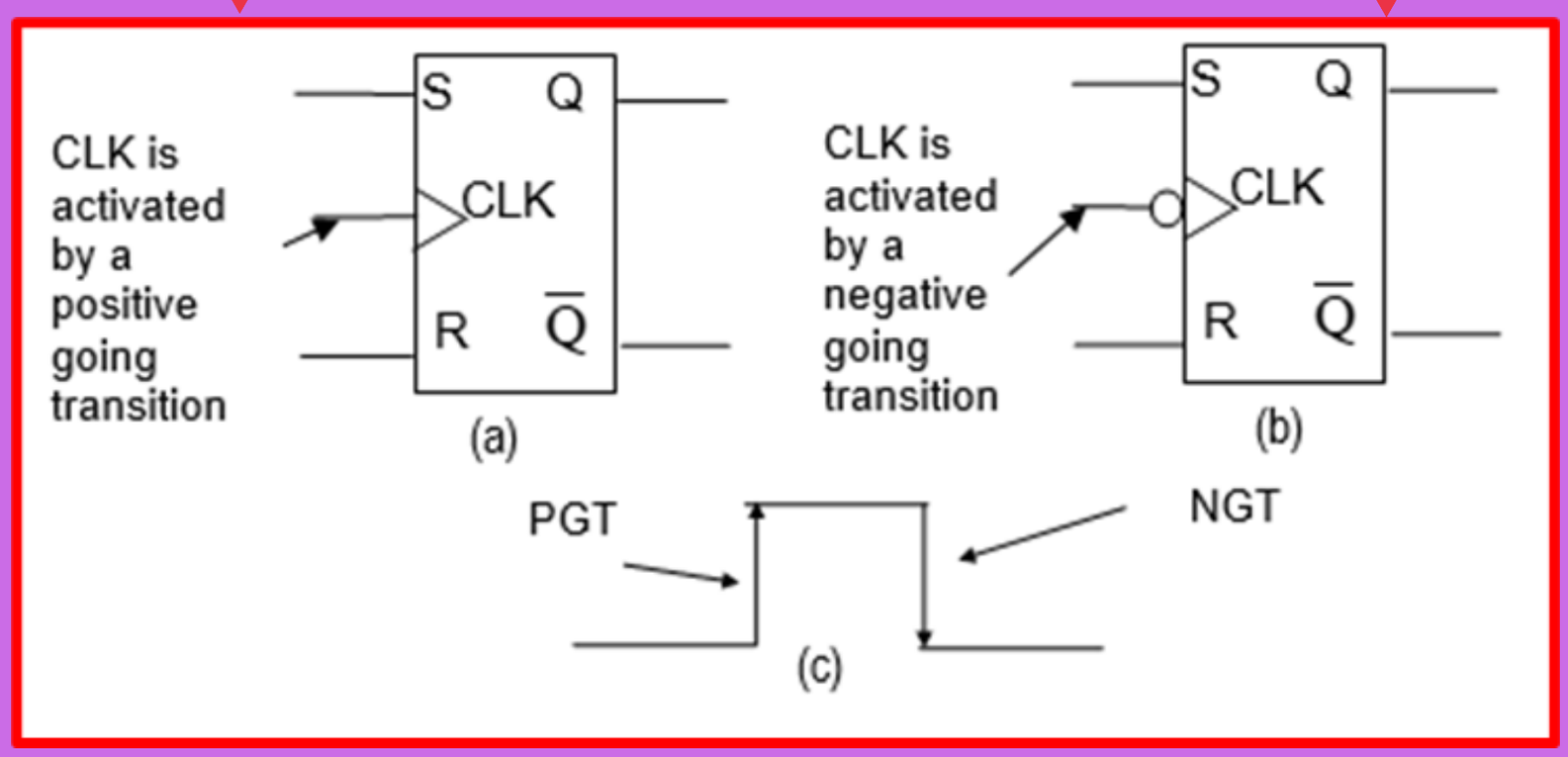
S	R	Q	$\bar{Q}$	OPERATION
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	0	1	No change

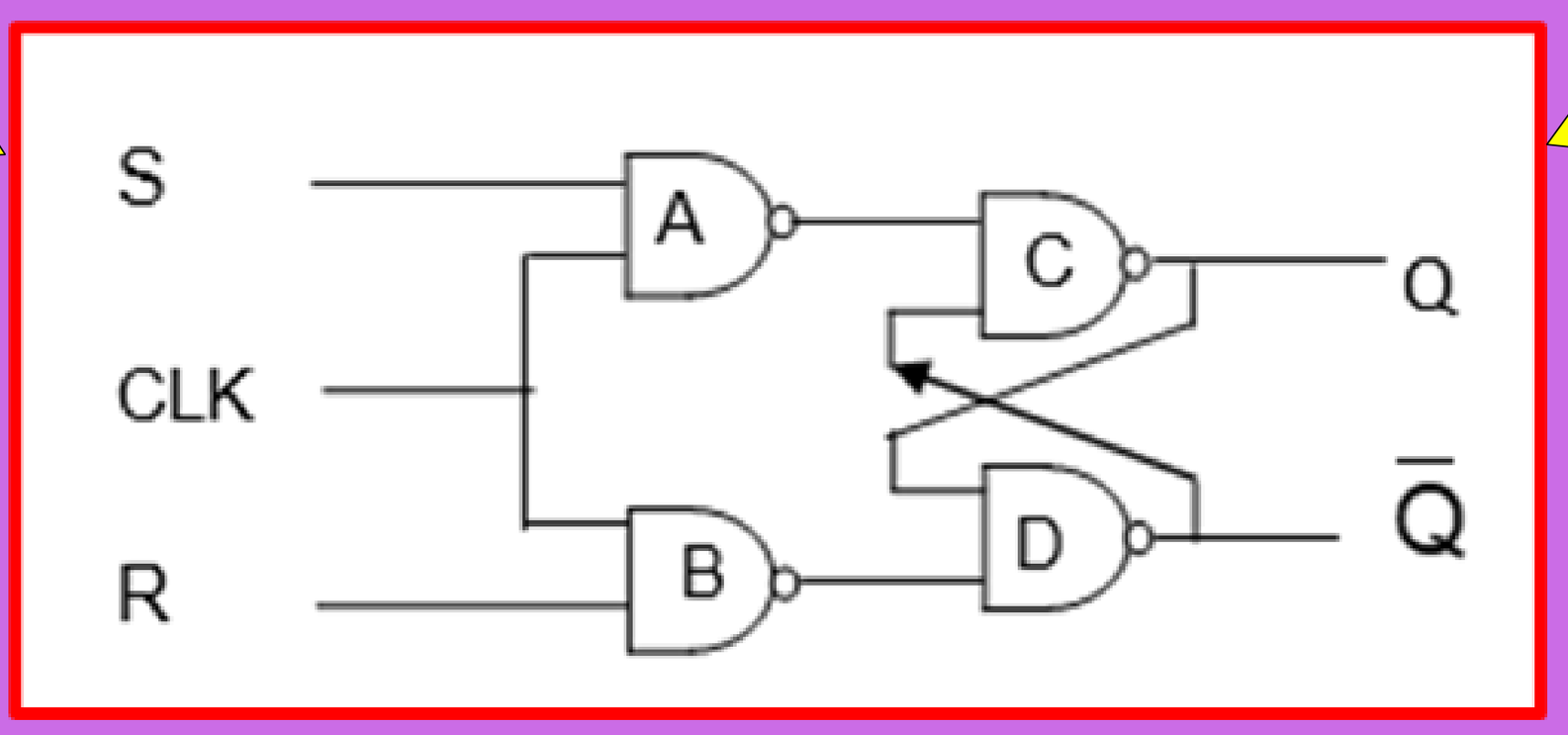


CLOCKED SR FLIP FLOP

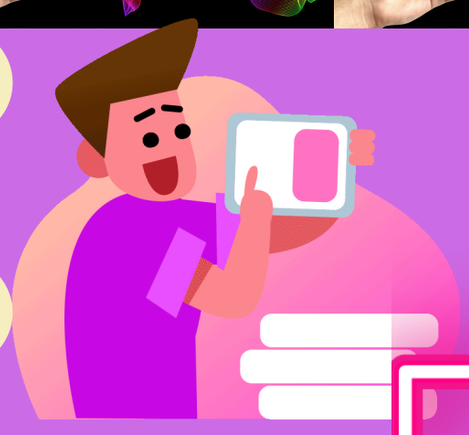
SR FLIP FLOP PGT

SR FLIP FLOP NGT

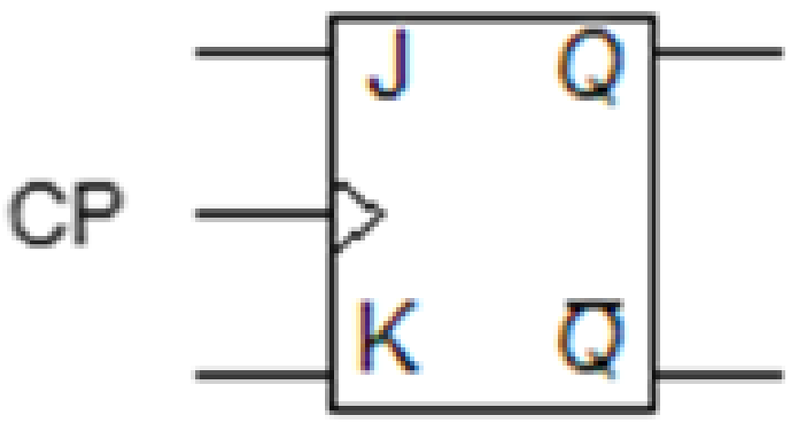


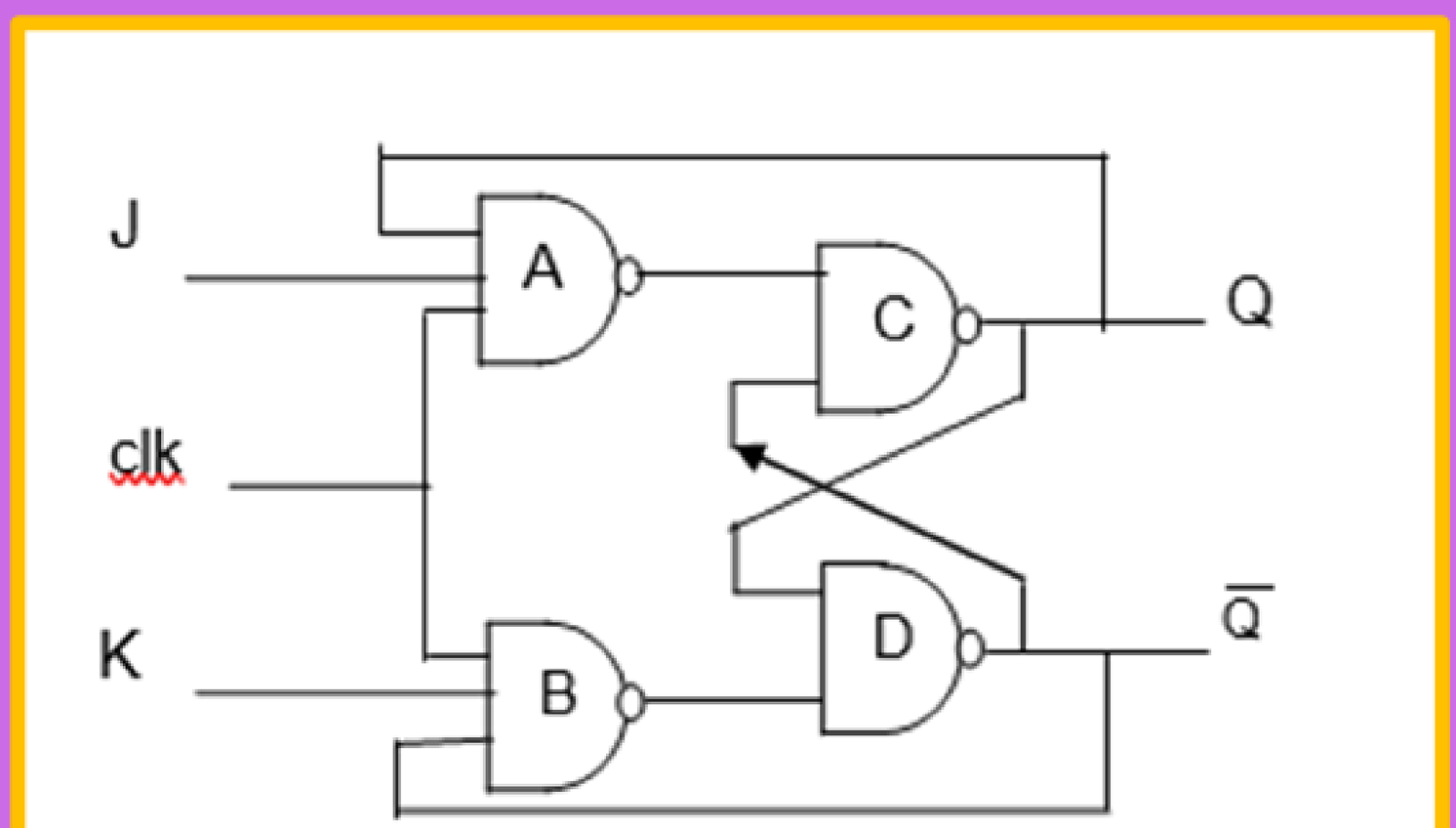


INPUT		OUTPUT		OPERATION
S	R	Q	Q'	
0	0	1/0	0/1	Hold
0	1	0	1	Reset
1	0	1	0	Set
1	1	1/0	1/0	Invalid

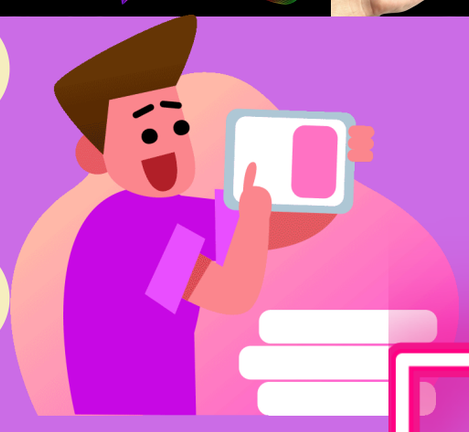


JK FLIP FLOP WITHOUT ASYNCHRONOUS INPUT

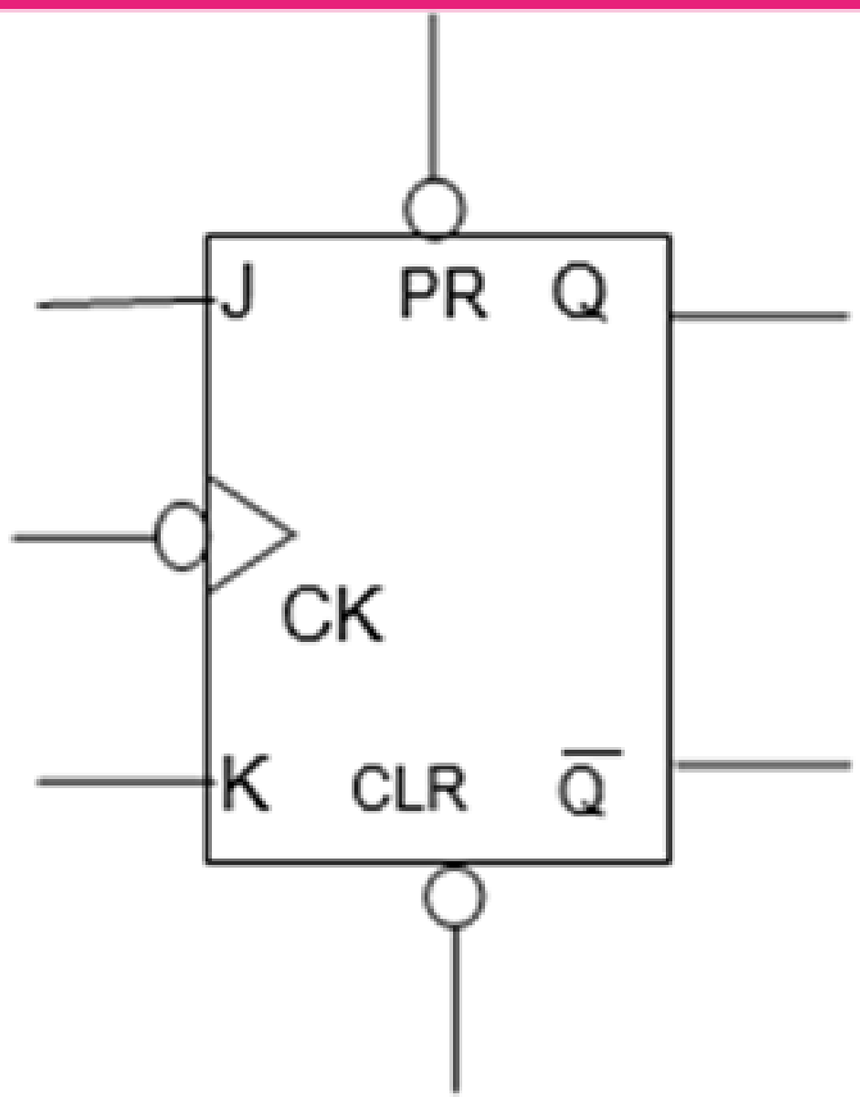




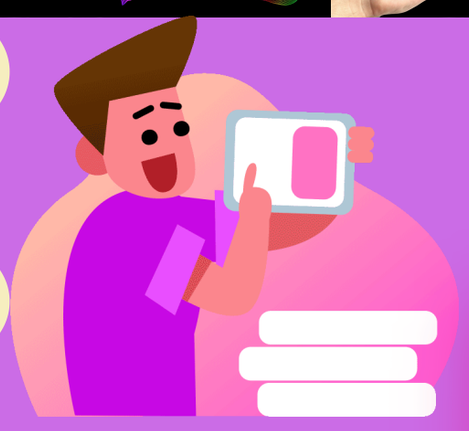
INPUT		OUTPUT		OPERATION
J	K	Q	Q'	
0	0	1/0	0/1	Hold
0	1	0	1	Reset
1	0	1	0	Set
1	1	1/0	0/1	Toggle



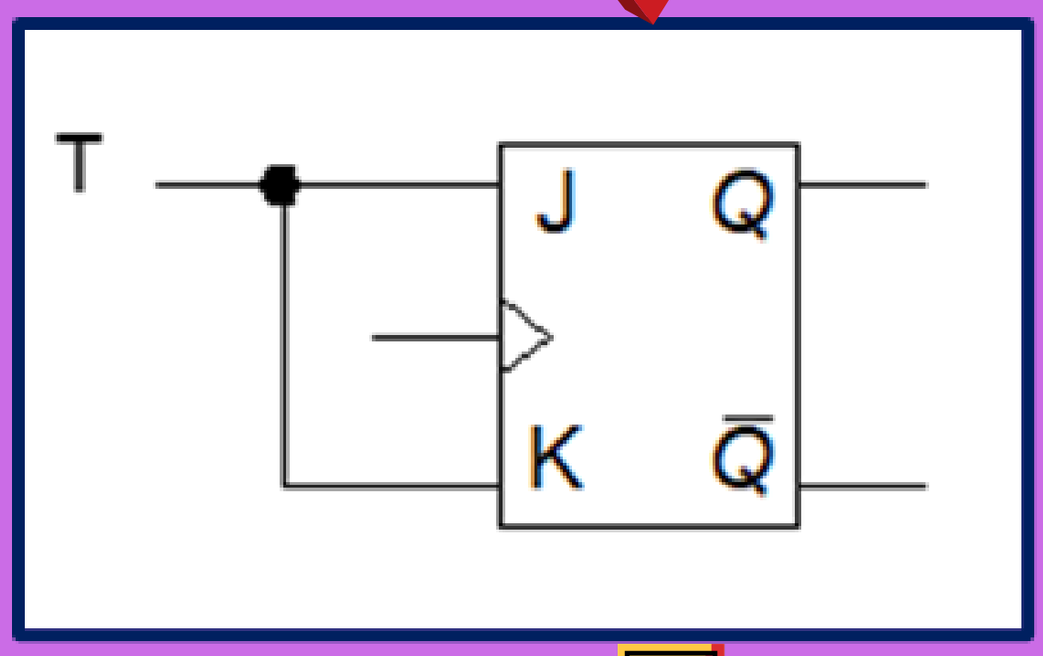
JK FLIP FLOP WITH ASYNCHRONOUS INPUT

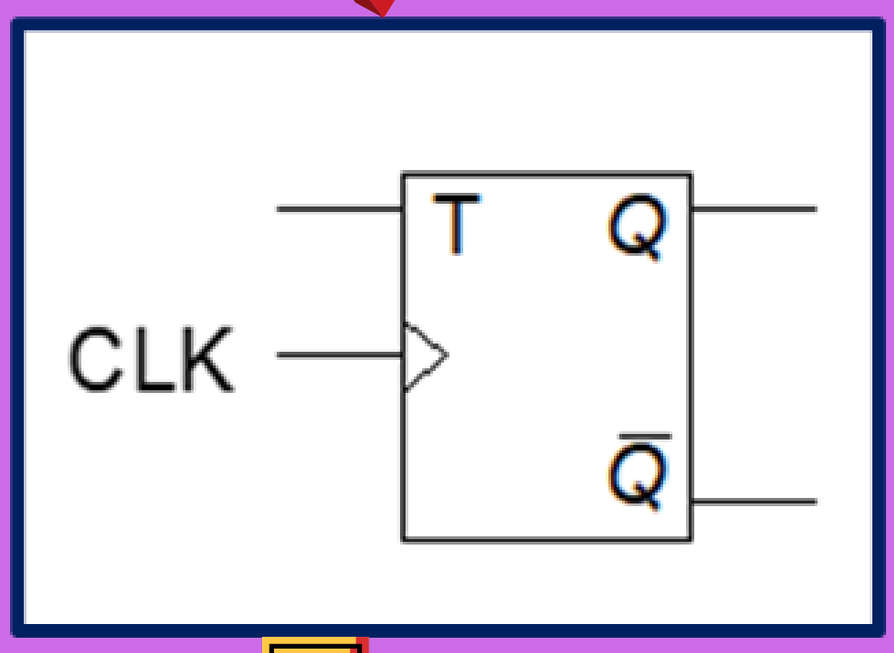


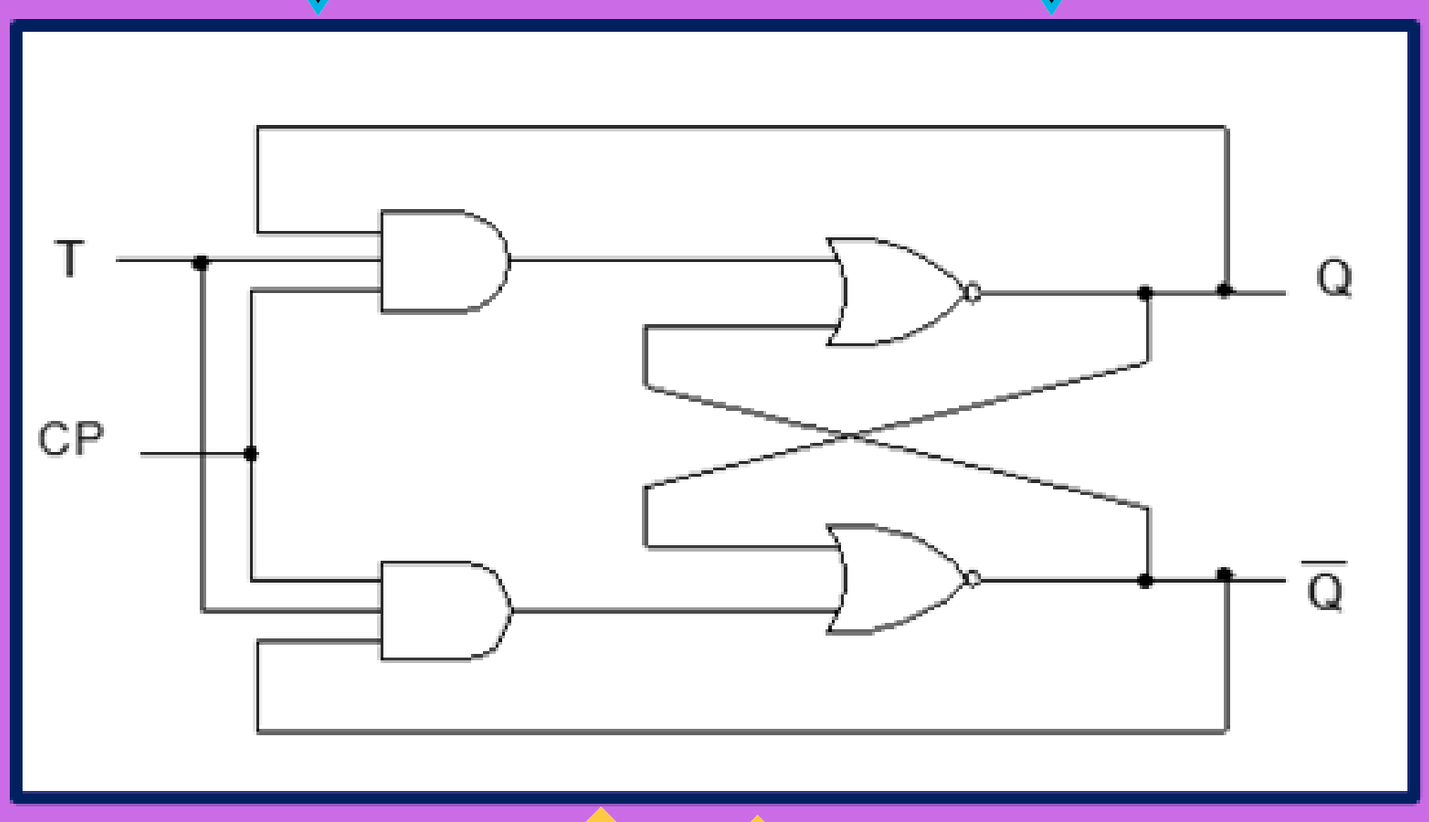
INPUT					OUTPUT		OPERATION
ASYNCHRONOUS		SYNCHRONOUS					
PRESET	CLEAR	J	K	CLK	Q	Q'	
0	1	X	X	X	1	0	ASYN SET
1	0	X	X	X	0	1	ASYN RESET
0	0	X	X	X	0/1	0/1	INVALID
1	1	0	0	⌐	0/1	1/0	HOLD
1	1	0	1	⌐	0	1	RESET
1	1	1	0	⌐	1	0	SET
1	1	1	1	⌐	0/1	1/0	TOGGLE



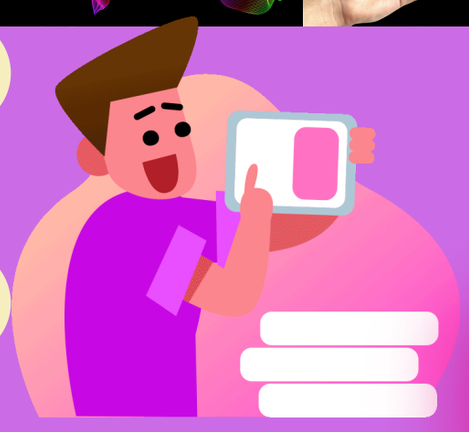
T FLIP FLOP



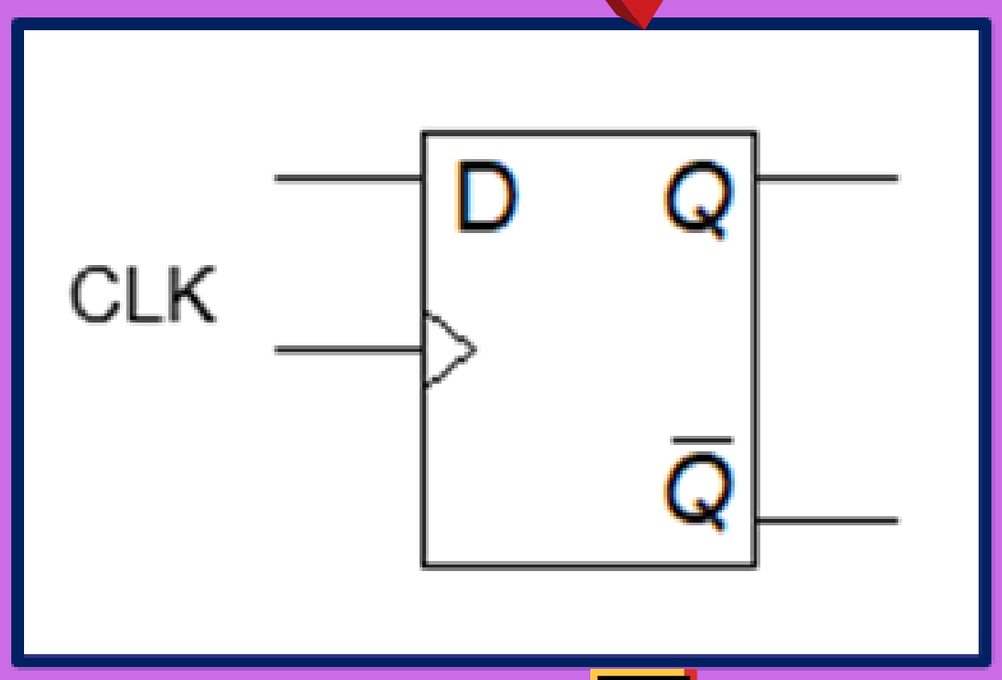


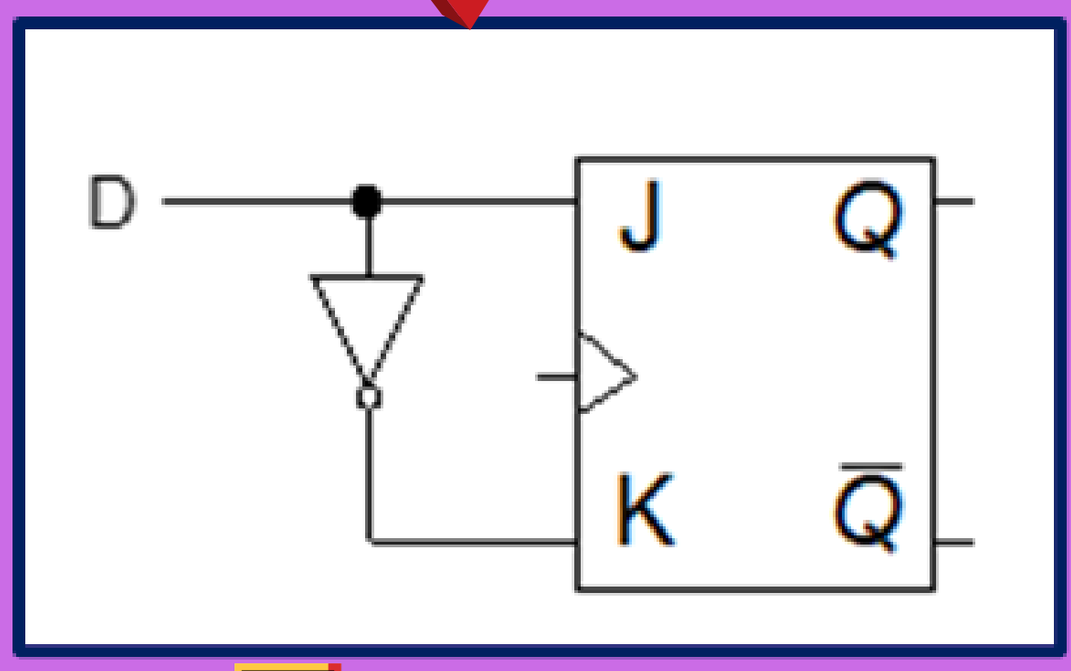


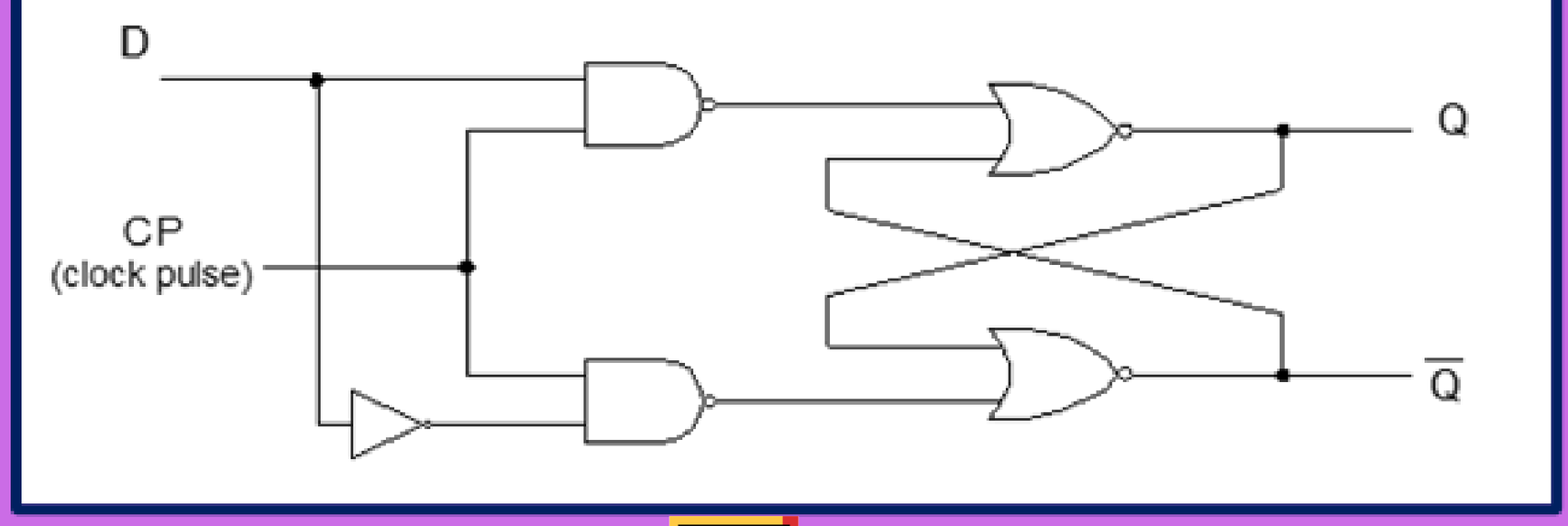
CLK	T	Q	Q′	Output State
(1)	0	0/1	1/0	No change
(1)	1	0/1	1/0	Toggle



D FLIP FLOP







CLK	D	Q	Q′	Output State
(1)	0	0	1	Store Data 0
(1)	1	1	0	Store Data 1

QUESTION 1

State FOUR(4) types of flip-flop.

QUESTION 2

State THREE(3) applications of flip-flop

QUESTION 3

Build the truth table of Clocked SR and JK flip-flop.

QUESTION 4

Draw a logic circuit of JK flip-flop and then convert the logic circuit to T flip-flop and D flip-flop.

QUESTION 5

State the output state for JK flip flop if the input and output are given in Table 4.

Table 4

CLK	J	K	Q	Q′	Output State
(1)	0	1	0	1	
-	1	1	0	1	
(1)	1	0	1	0	
(1)	1	1	0	1	

QUESTION 6

Identify the type and construct the truth table of flip-flop shown in Figure 5.

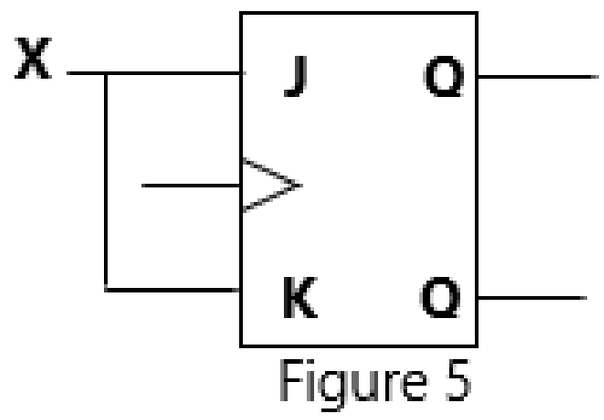


Figure 5

QUESTION 7

Identify the input for T flip-flop for toggle mode.

QUESTION 8

Draw the output waveform, Q and Q'for JK flip-flop positive edge trigger in Figure 8. Initial Q = 0

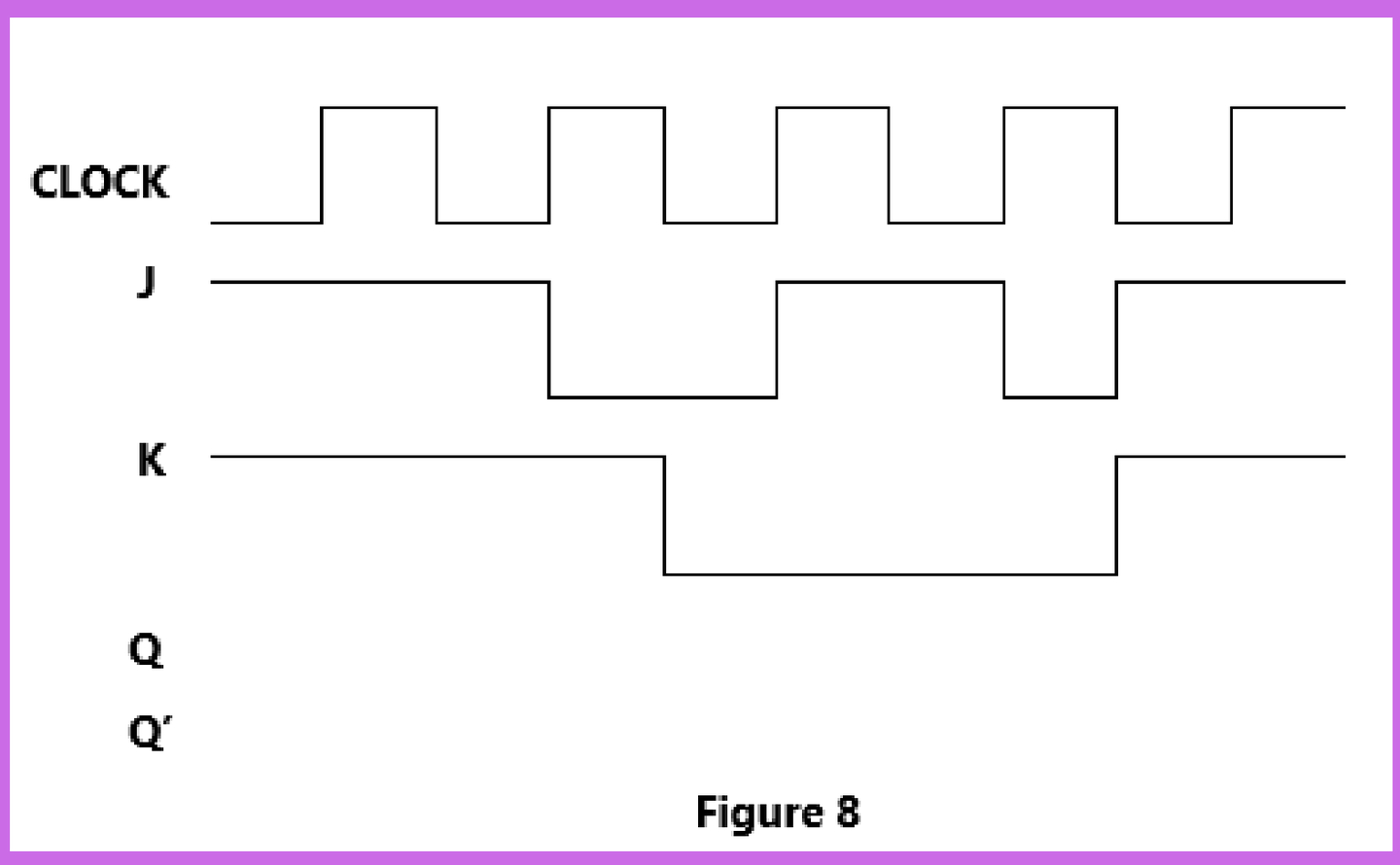


Figure 8

QUESTION 9

Draw the output waveform, Q and Q' for D flip-flop negative edge trigger in Figure 8. Initial Q = 1

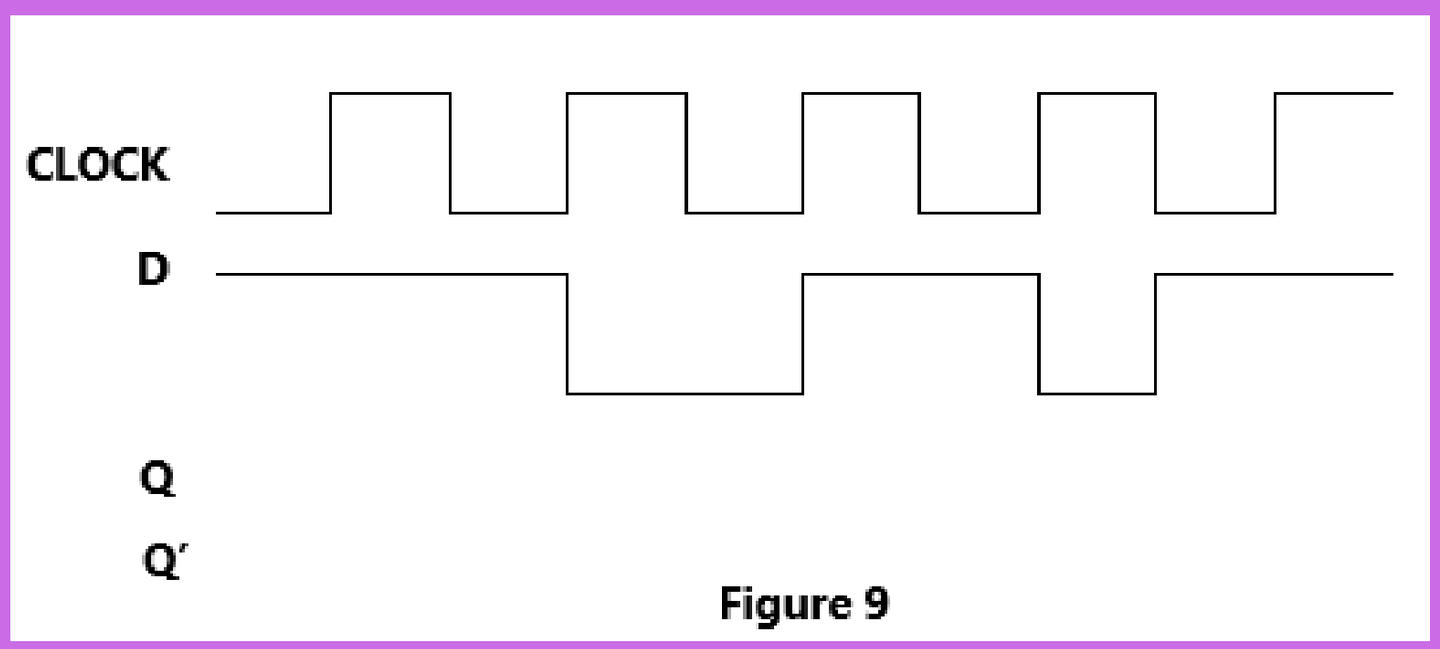


Figure 9

QUESTION 10

Identify the input for JK flip-flop for no change mode.

ANSWER 1

SR flip-flop, JK flip-flop, T flip-flop, D flip-flop.

ANSWER 2

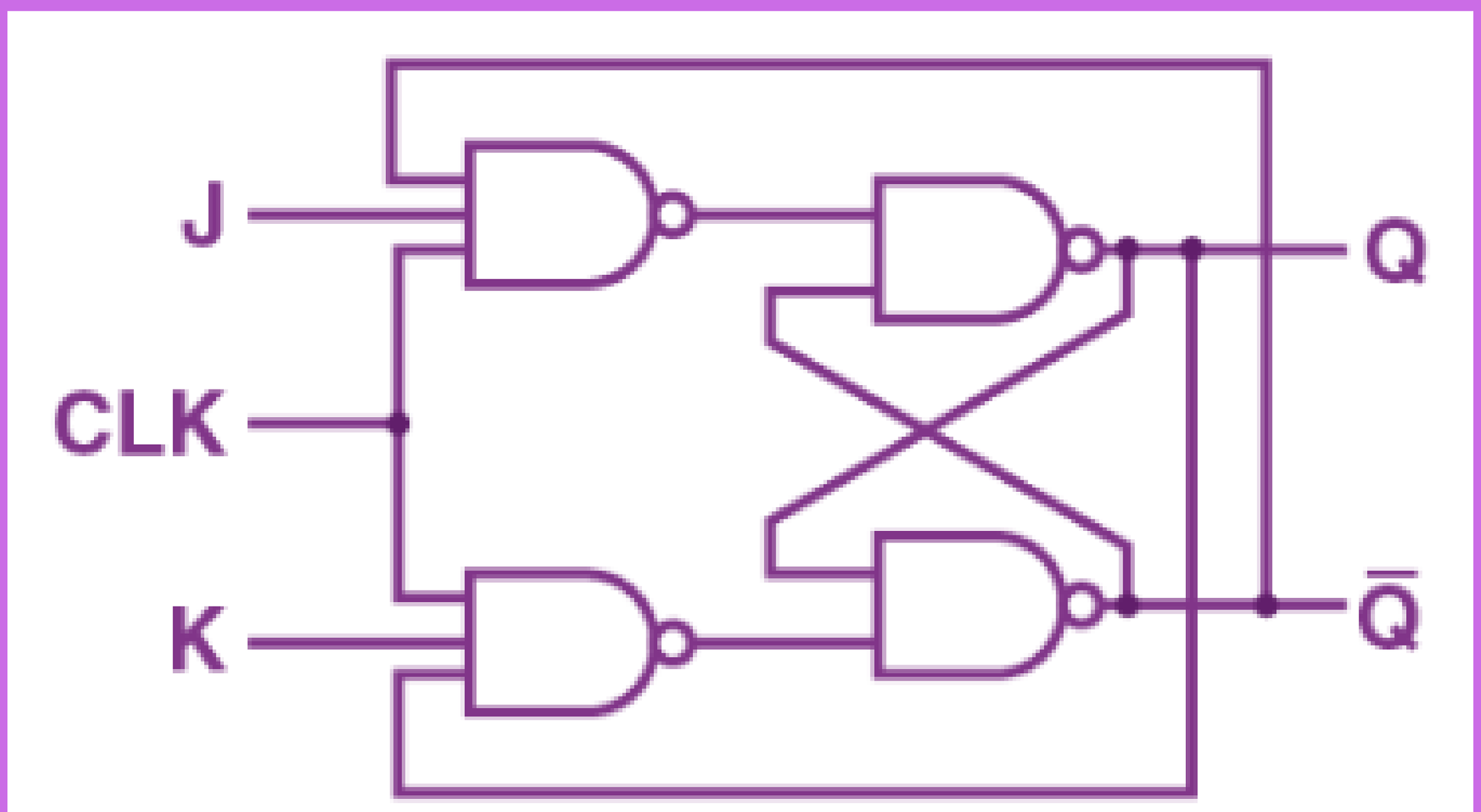
Frequency divider, Counters, Shift registers, Data storage, Memory,

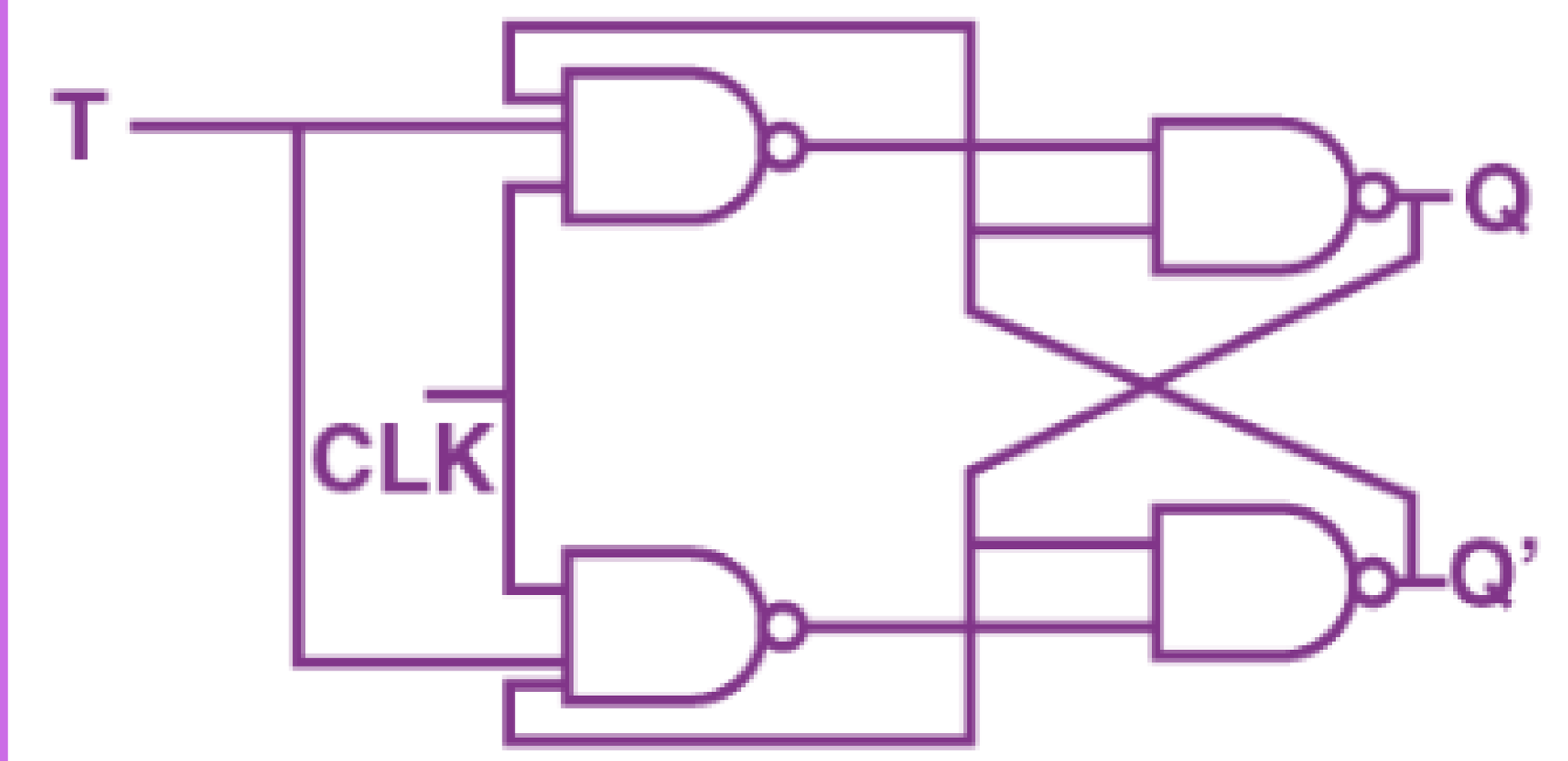
ANSWER 3

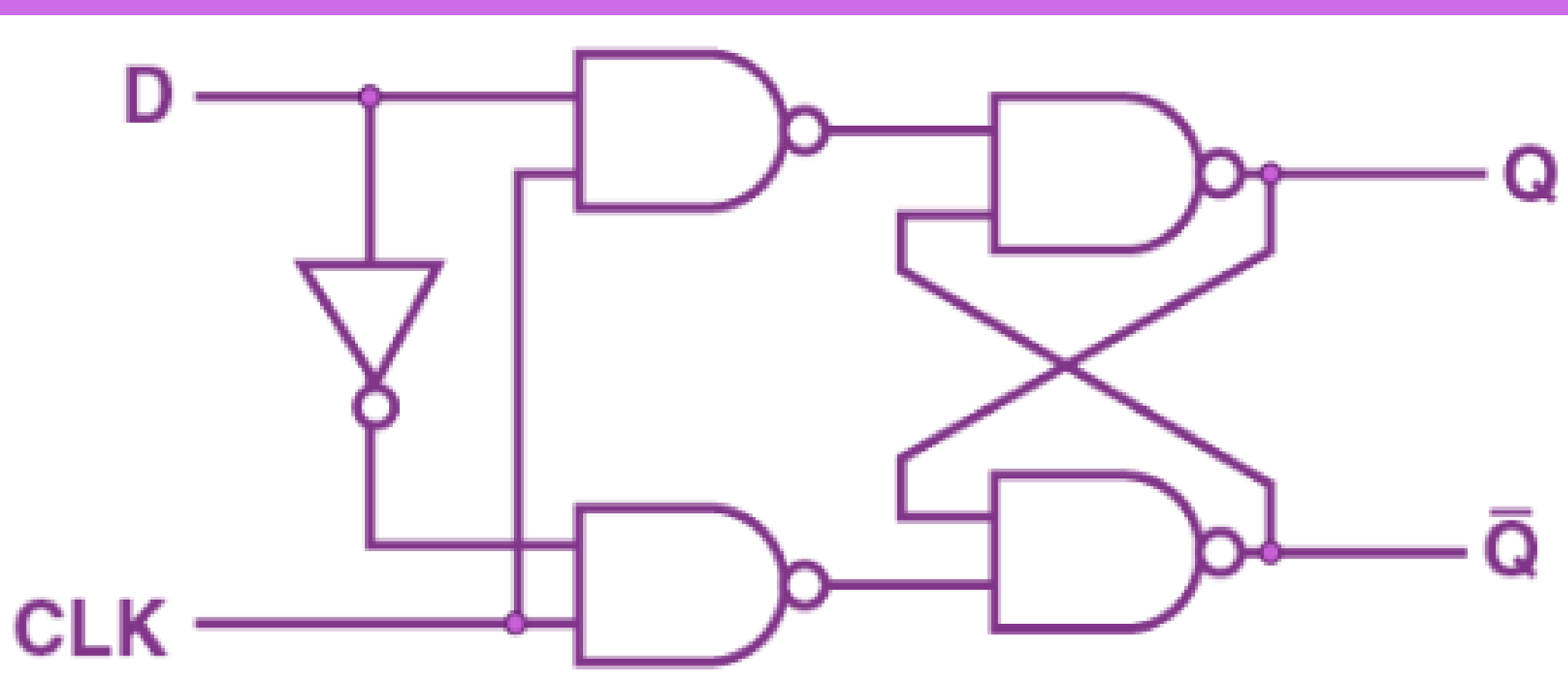
CLK	S	R	Q	Q′	Output State
(1)	0	0	0/1	1/0	No change
(1)	0	1	0	1	Reset
(1)	1	0	1	0	Set
(1)	1	1	0/1	0/1	Invalid

CLK	J	K	Q	Q′	Output State
(1)	0	0	0/1	1/0	No change
(1)	0	1	0	1	Reset
(1)	1	0	1	0	Set
(1)	1	1	0/1	1/0	Toggle

ANSWER 4







ANSWER 5

Reset
No Change
Set
Toggle

ANSWER 6

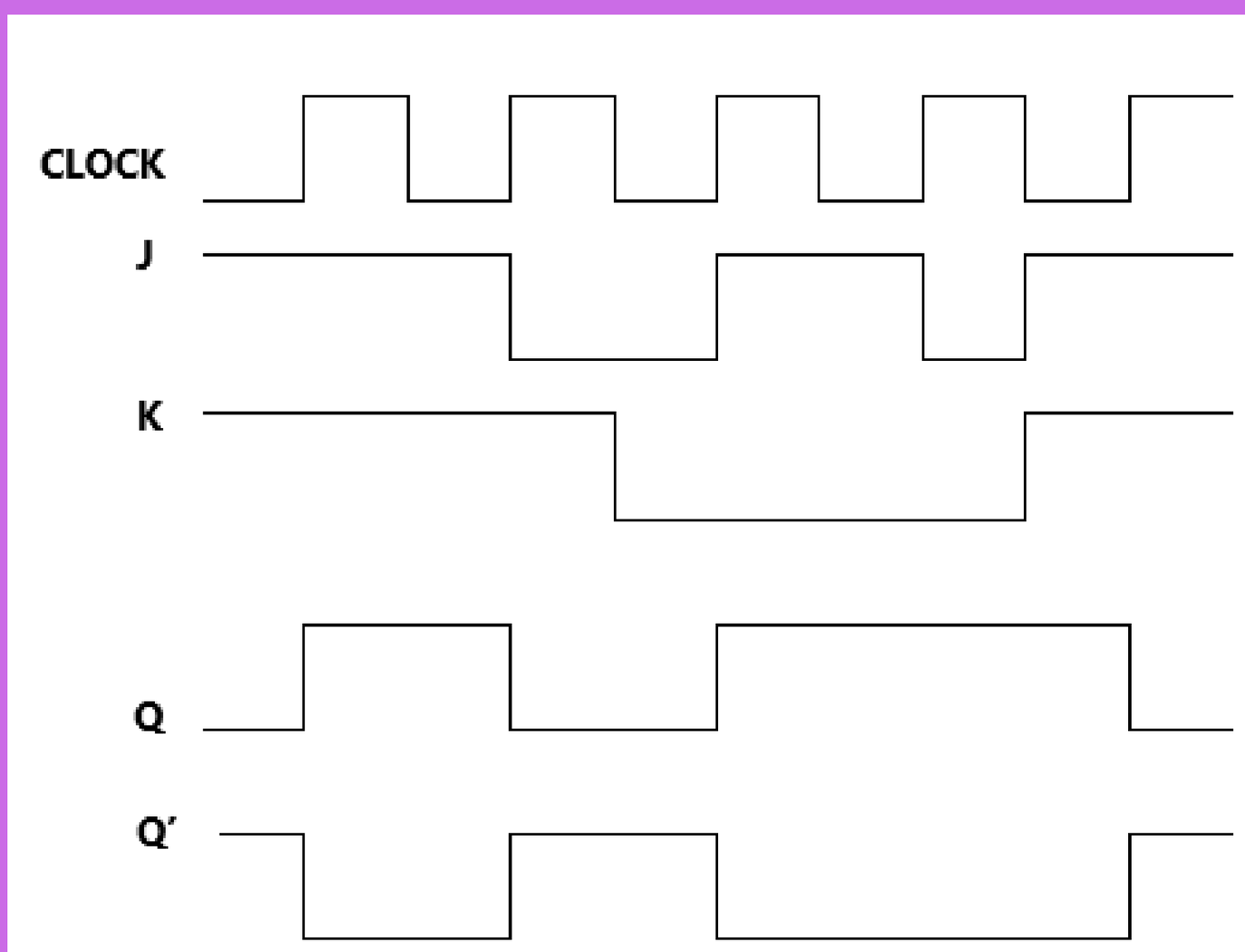
T flip-flop

CLK	T	Q	Q′	Output State
(1)	0	0/1	1/0	No change
(1)	1	0/1	1/0	Toggle

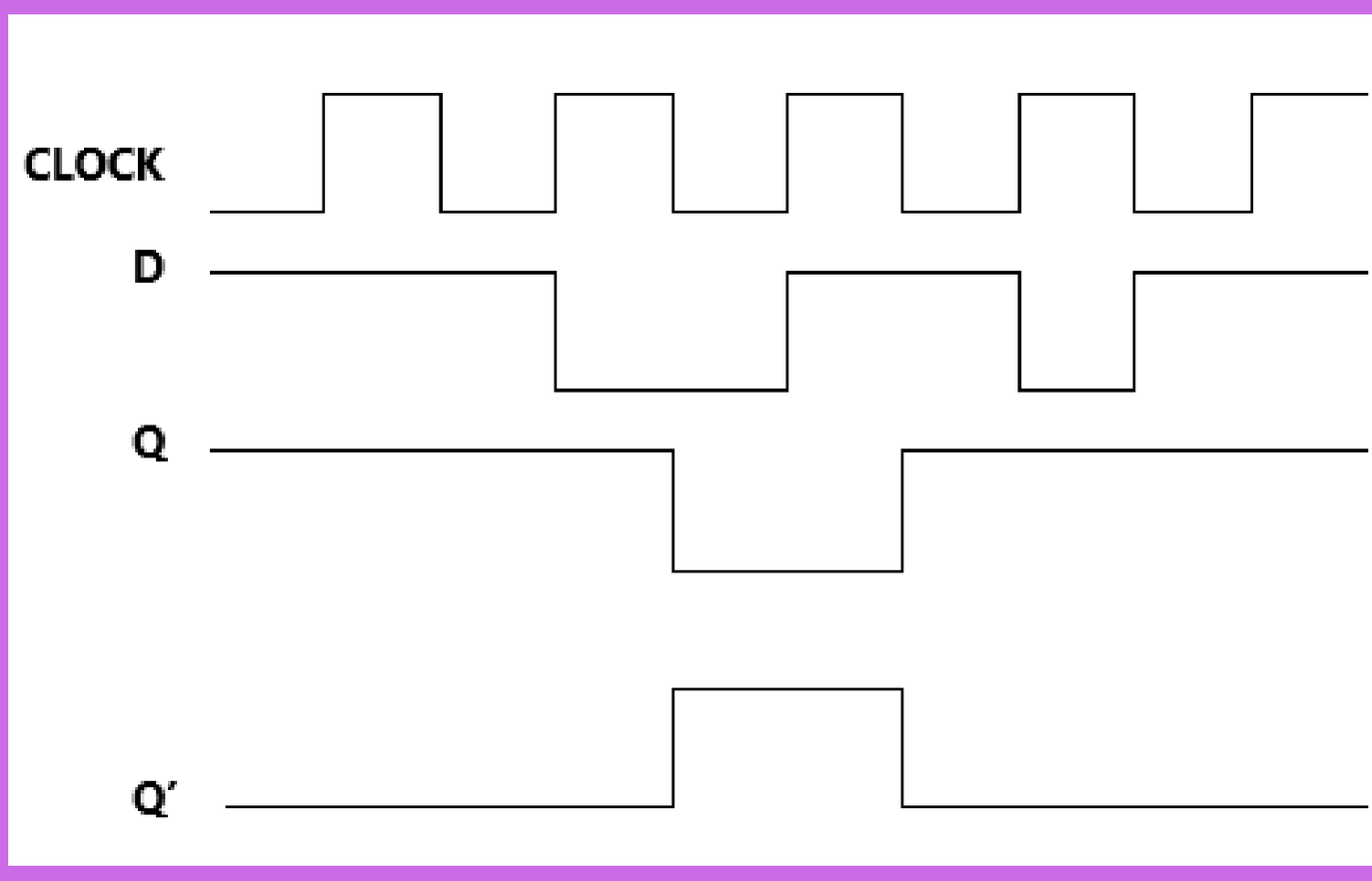
ANSWER 7

T = 1

ANSWER 8



ANSWER 9

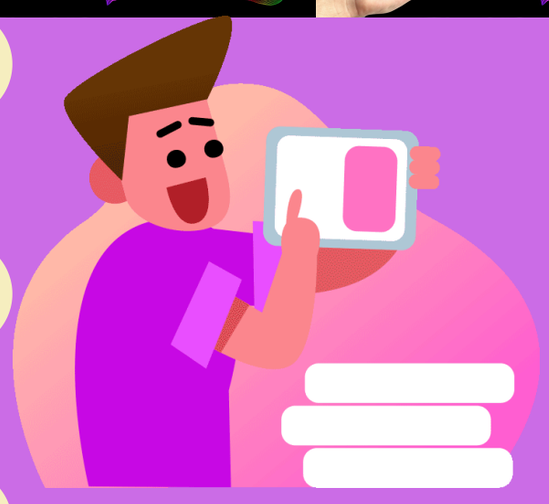


ANSWER 10

J = 0, K= 0

Chapter 4

Counters



COUNTER

ASYNCHRONOUS COUNTER

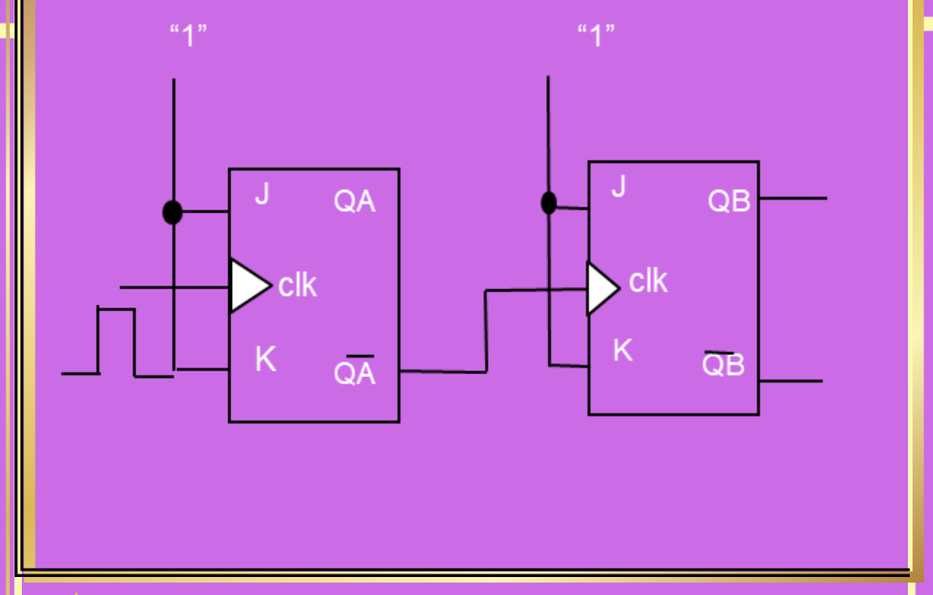
SYNCHRONOUS COUNTER

DIFFERENCES

HIGH PROPAGATION DELAY

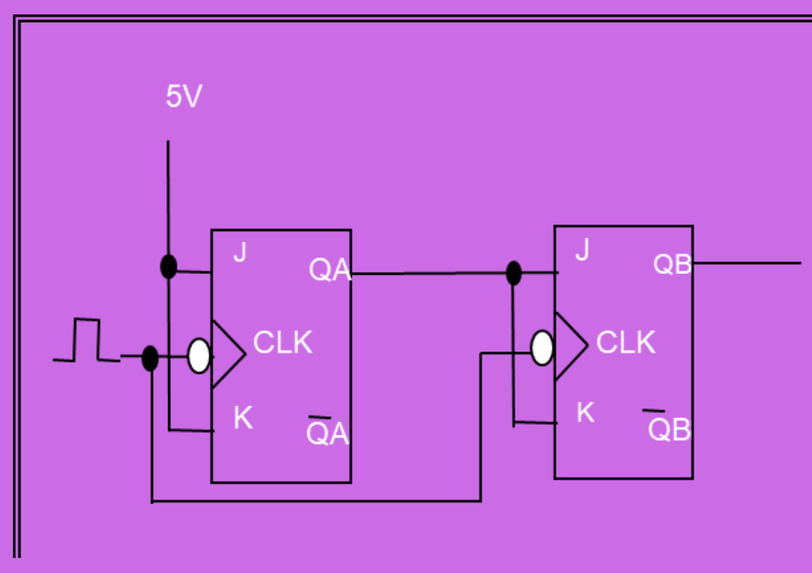
LOW PROPAGATION DELAY

SIMPLE CIRCUIT

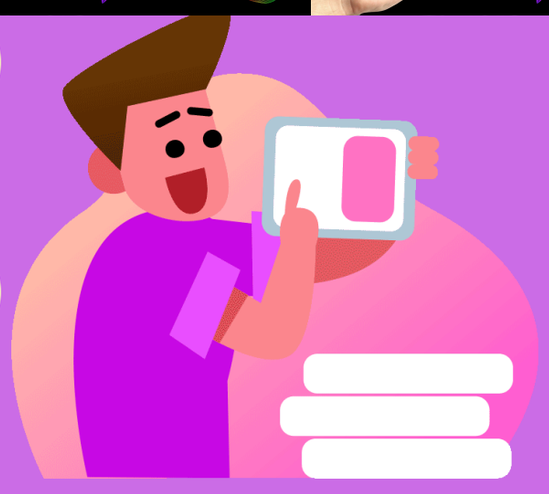


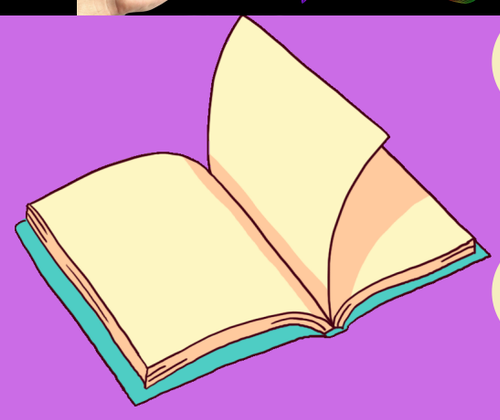
COMPLEX CIRCUIT

COUNT CONSECUTIVELY



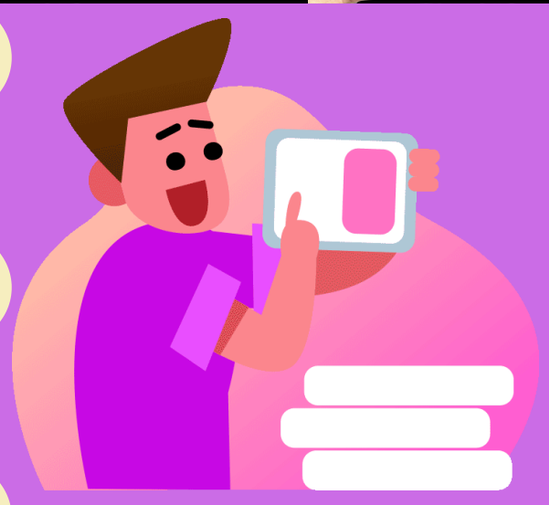
CAN COUNT RANDOM

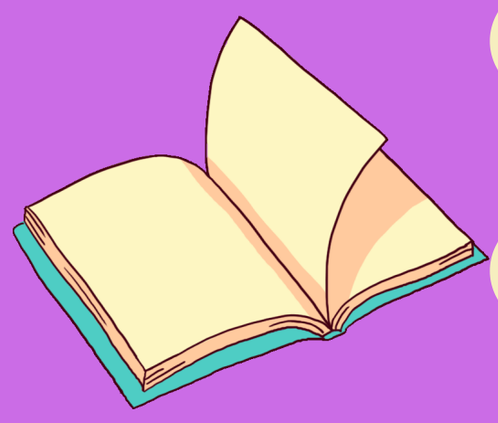




METHODS TO DESIGN ASYNCHRONOUS COUNTER

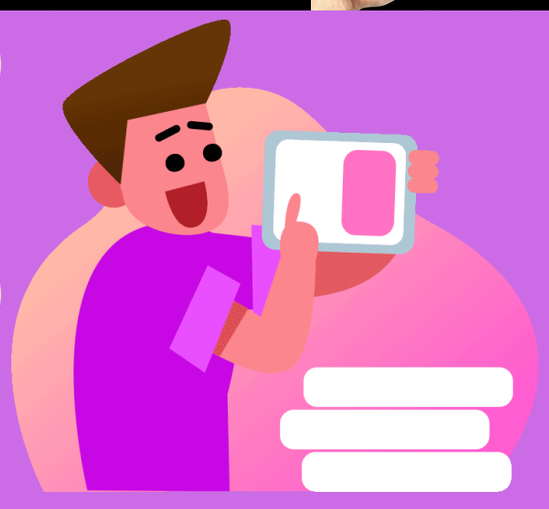
1. GET THE NUMBER OF FLIP FLOP NEEDED (LOG N/LOG 2)
2. GET THE LARGEST DECIMAL NUMBER (N-1)
3. DRAW STATE DIAGRAM
4. BUILD COUNTER CIRCUIT





Methods to design Asynchronous counter N<2^n

1. GET THE NUMBER OF FLIP FLOP NEEDED (LOG N/LOG 2)
2. GET THE LARGEST DECIMAL NUMBER (N-1)
3. DRAW STATE DIAGRAM
4. BUILD ASYNCHRONOUS COUNTER CIRCUIT
5. DETERMINE FLIP FLOP OUTPUT WITH LOGIC 1 AND CONNECT TO NAND GATE INPUT. NAND GATE OUTPUT WILL CONNECT TO CLEAR INPUT OF ALL FLIP FLOP



METHODS TO DESIGN SYNCHRONOUS COUNTER

1. DETERMINE FLIP FLOP NUMBER OF NECESSITY (LOG M+1/LOG 2), M = MAXIMUM NUMBER
2. DRAW STATE DIAGRAM
3. FILL IN EXCITATION TABLE
4. GET THE EQUATION USING KARNAUGH MAP
5. BUILD COUNTER CIRCUIT

QUESTION 1

Construct the state diagram for synchronous counter that will count number from 0,2,4,6,8.

QUESTION 2

State TWO(2) advantages of synchronous counter.

QUESTION 3

Construct 2-bit asynchronous up counter using JK flip-flop negative edge trigger.

QUESTION 4

A Mod-2 and Mod-4 counter are cascaded. Determine the output frequency if the input clock frequency is 60MHz.

QUESTION 5

Calculate the number of flip-flop needed to design a counter that counts the sequence of 6,4,2,3 repeatedly.

QUESTION 6

Design a synchronous up counter circuit that will count the random number 1,2,5,7 repeatedly by using positive edge triggerred JK flip-flop

QUESTION 7

Design a synchronous up counter circuit Mod-3 using negative edge triggered T flip-flop.

QUESTION 8

Design an asynchronous down counter circuit Mod-8 using negative edge triggered T flip-flop.

QUESTION 9

Design an asynchronous up counter Mod-9 using negative edge triggered JK flip-flop .

QUESTION 10

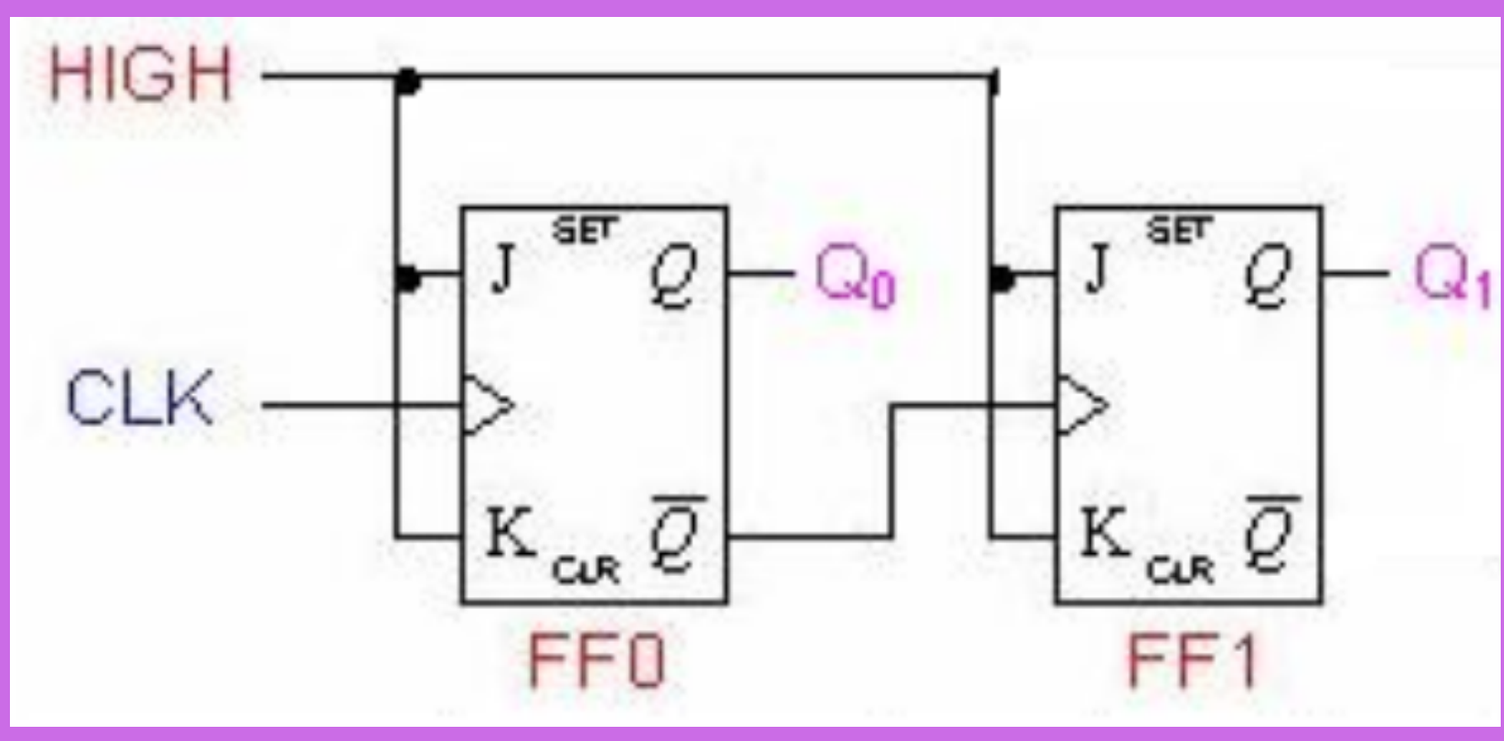
Design a synchronous counter circuit that will count 1,3,4,6 repeatedly using negative edge triggered JK flip-flop.

ANSWER 1

ANSWER 2

- Low propagation delay
- Can count randomly

ANSWER 3



ANSWER 4

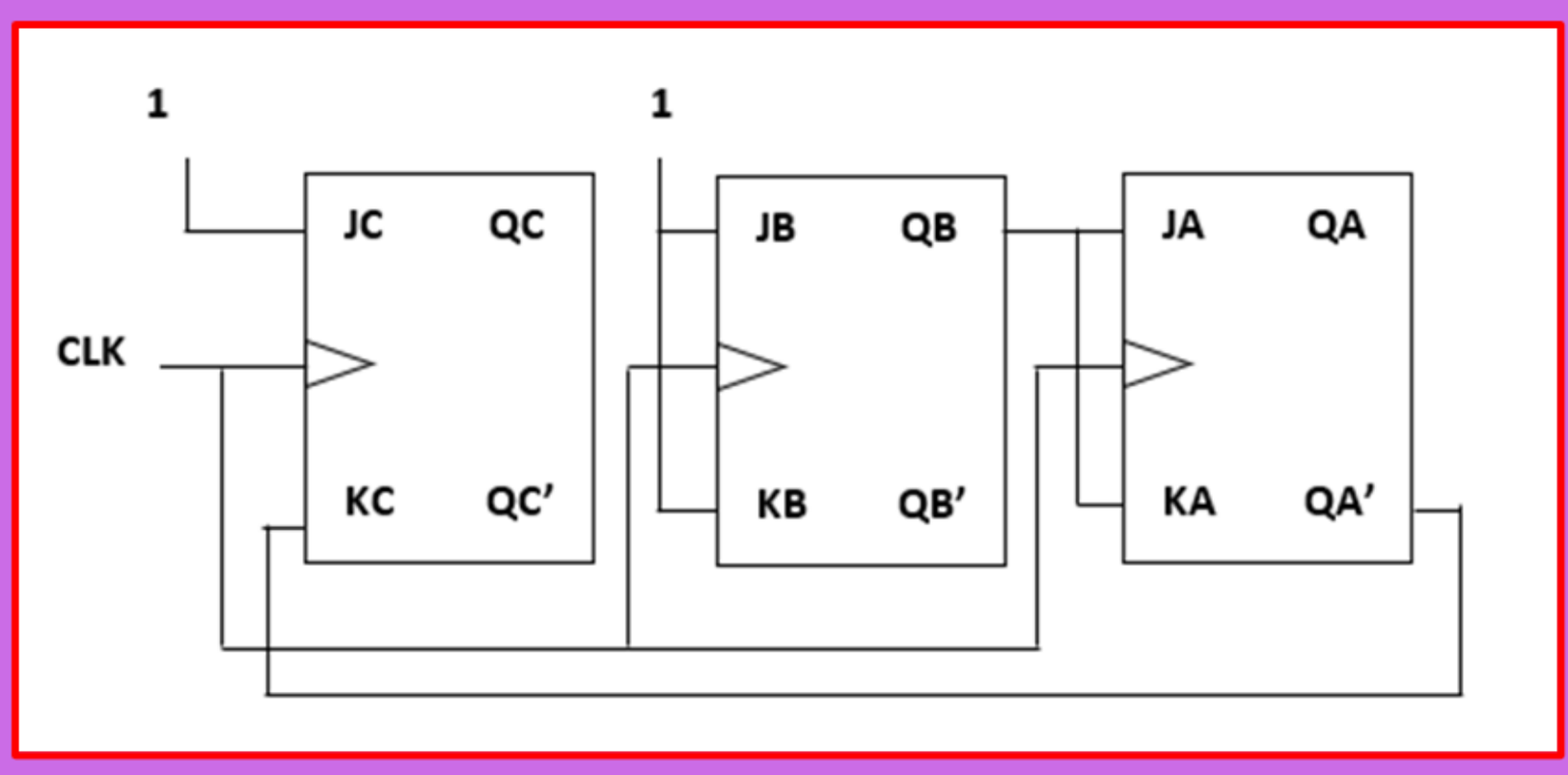
234375 Hz

ANSWER 5

3 FF

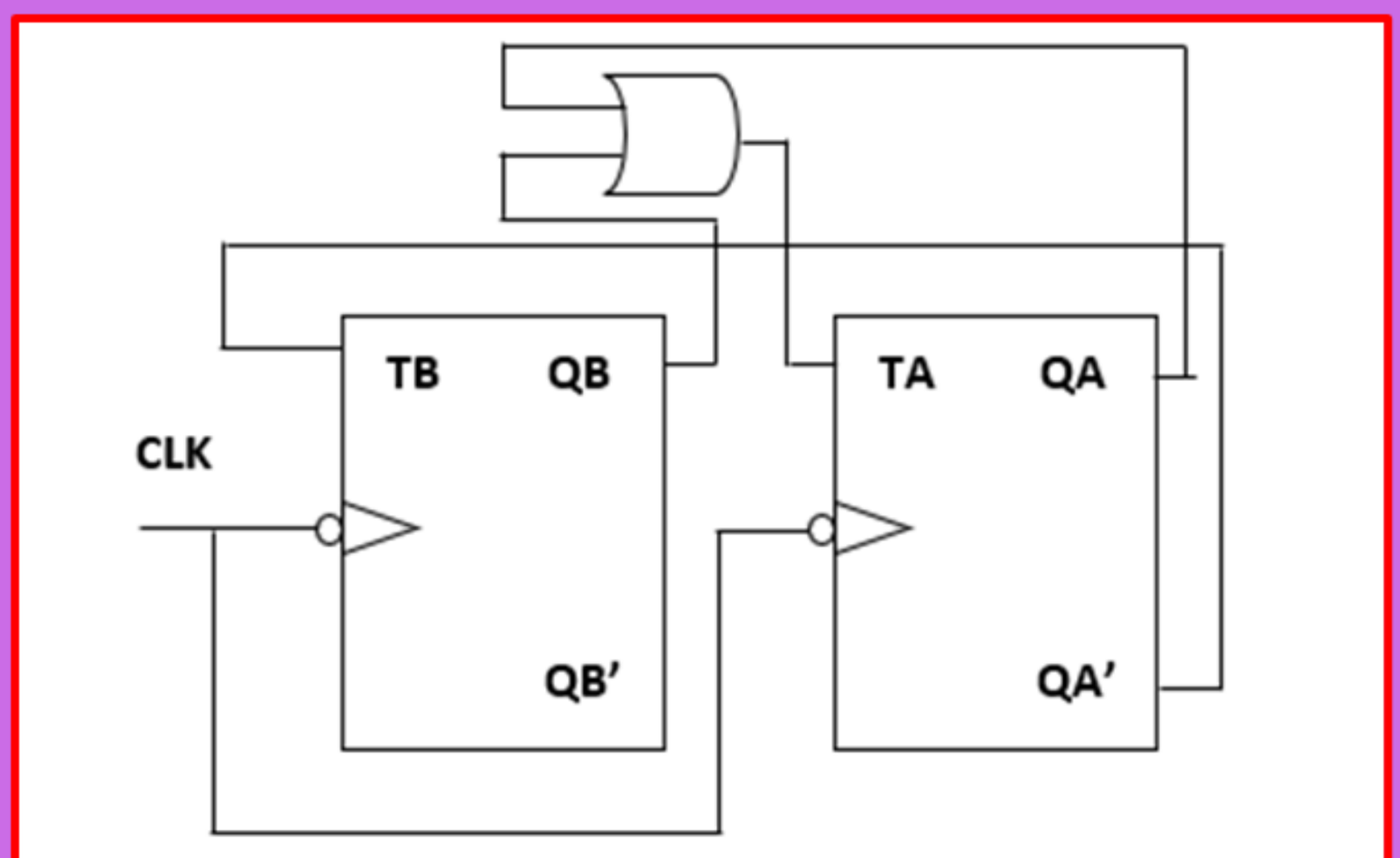
ANSWER 6

JA = C' @A
KA = B
JB = 1
KB = 1
JC = 1
KC = A'

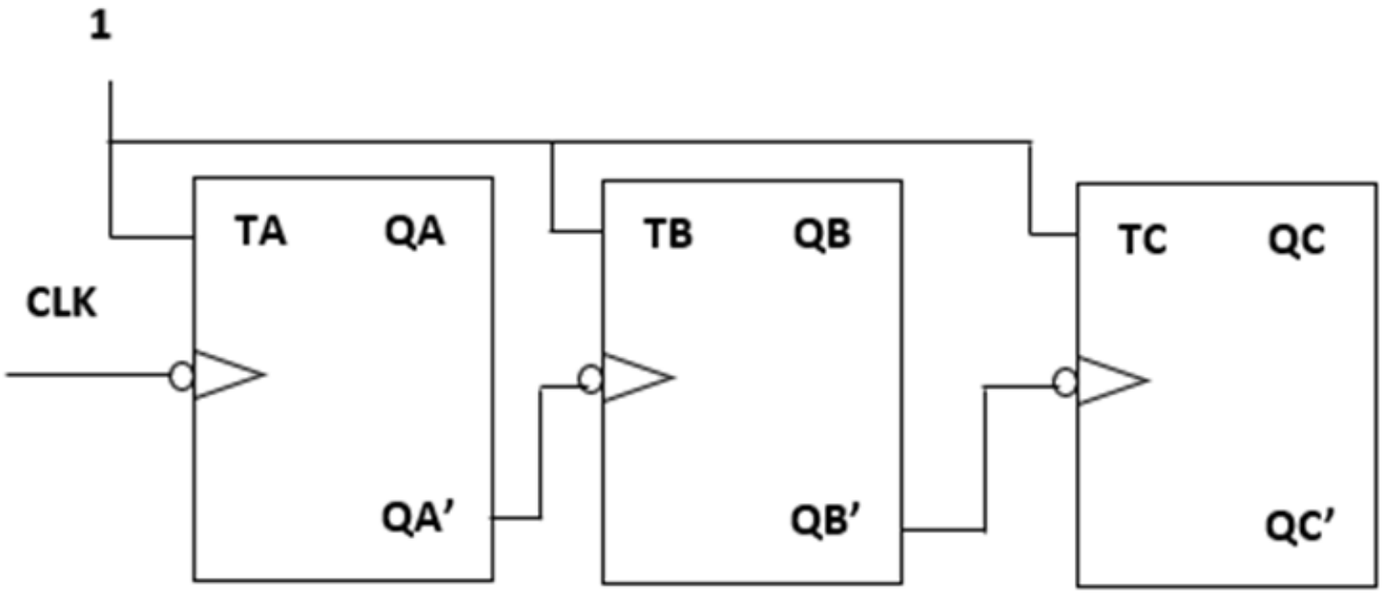


ANSWER 7

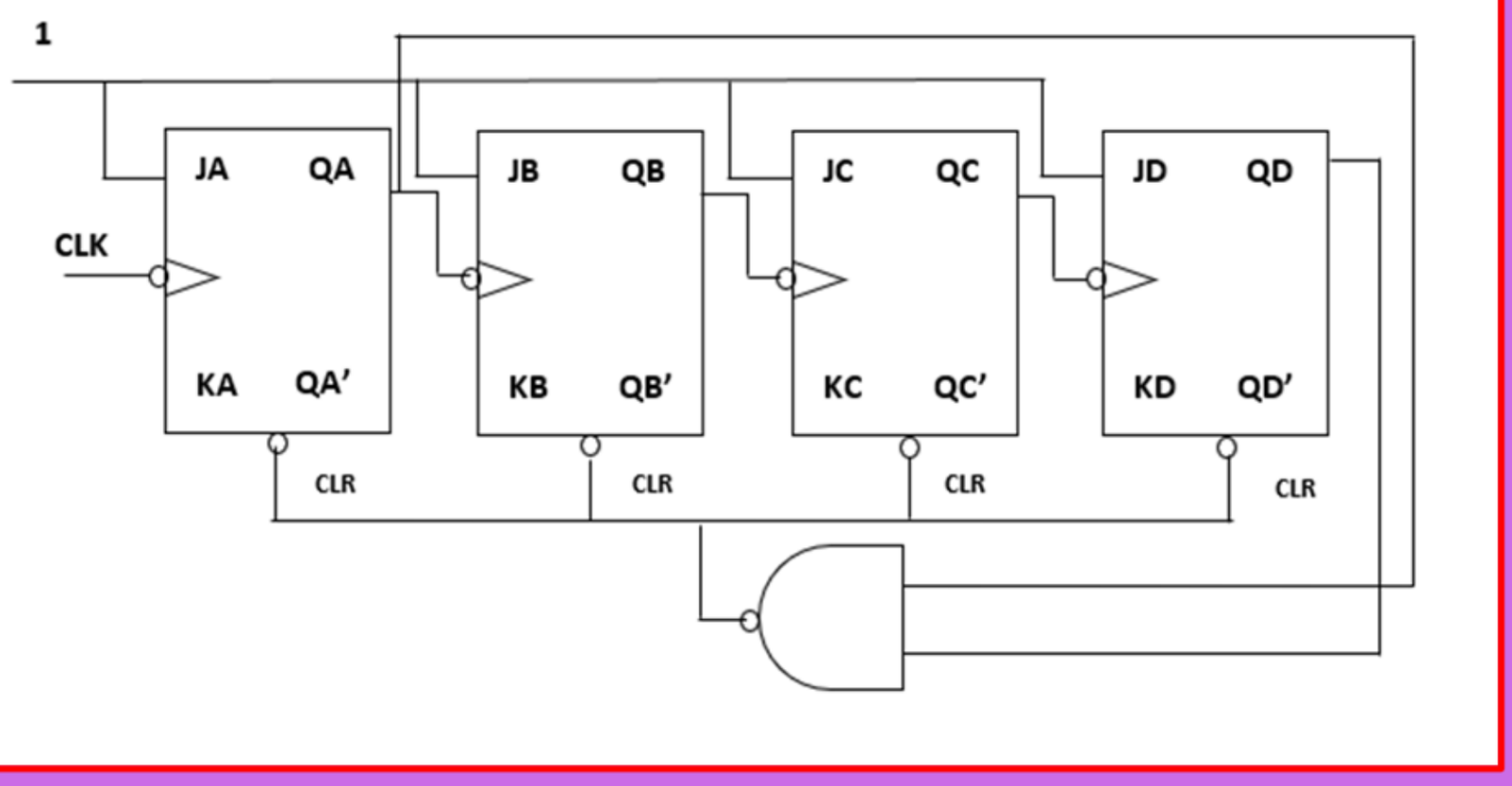
TA = B+A
TB = A'



ANSWER 8

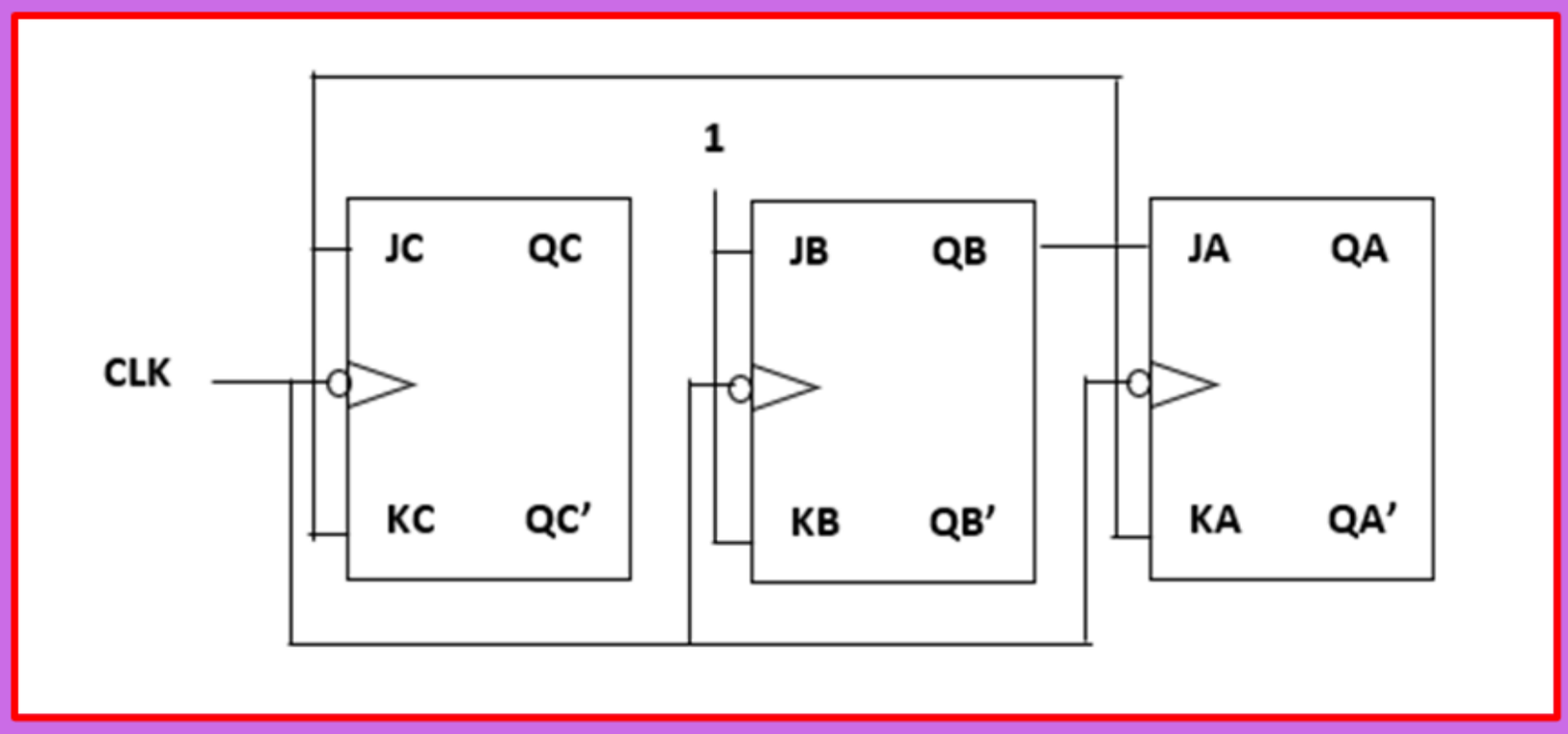


ANSWER 9



ANSWER 10

JA = B KA = B JB = 1 KB = 1
JC = B KC = B



Chapter 5

Registers

REGISTER

CONCEPT

A shift register is a sequential logic circuit that acts as a unit to store and transfer binary data

TYPES OF REGISTER

- SISO
- SIPO
- PISO
- PIPO

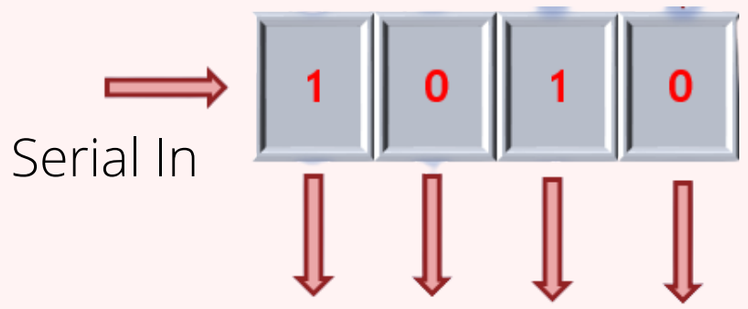
APPLICATION

- Arithmetic
  - Multiple
  - Divider
- Shift Register Counter
  - Ring Counter
  - Johnson Counter

Types of Register

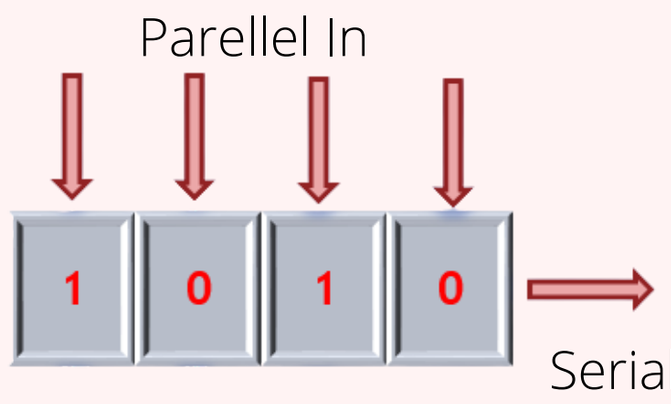
Notes!
S - Serial
P - Parallel
I - In
O - Out

SIPO



SIPO's Concept:
Shifted data enter a bit at every time, after bit altogether included, it would be shifted out simultaneously

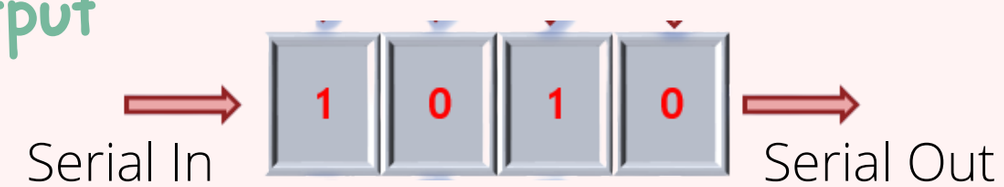
PISO



PISO'S Concept:
Bit altogether data in enter simultaneously, and shift out a bit at every time.

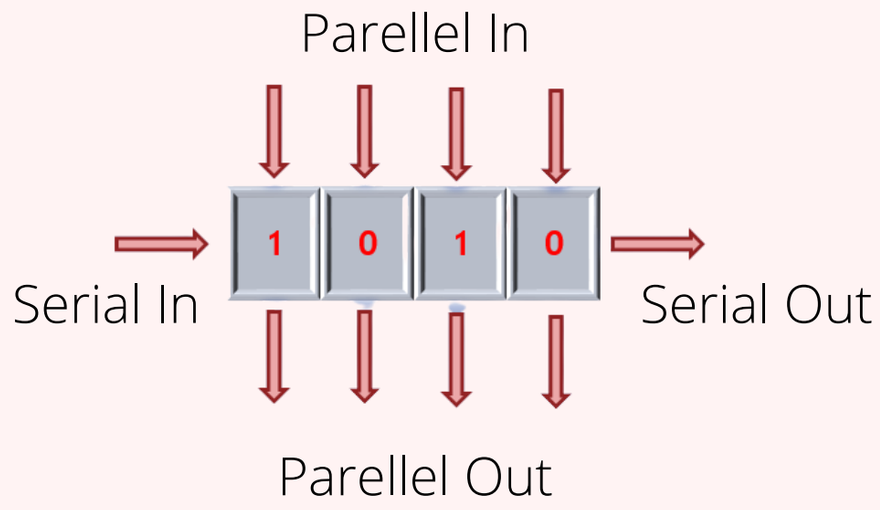
SISO

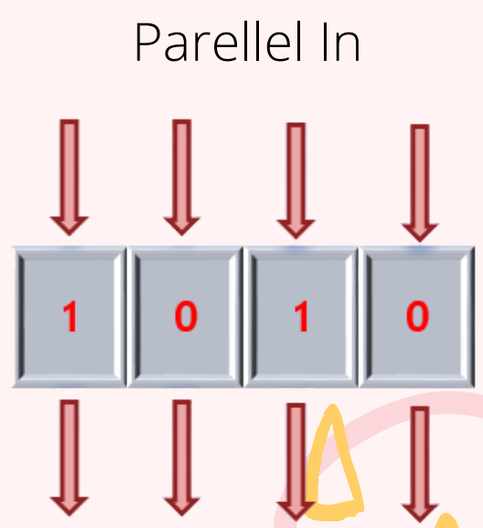
SISO's Concept:
Data shifted in and out one bit each time through one input and line output



PIPO

PIPO's Concept:
Bit altogether data in enter simultaneously, and shit out simultaneously





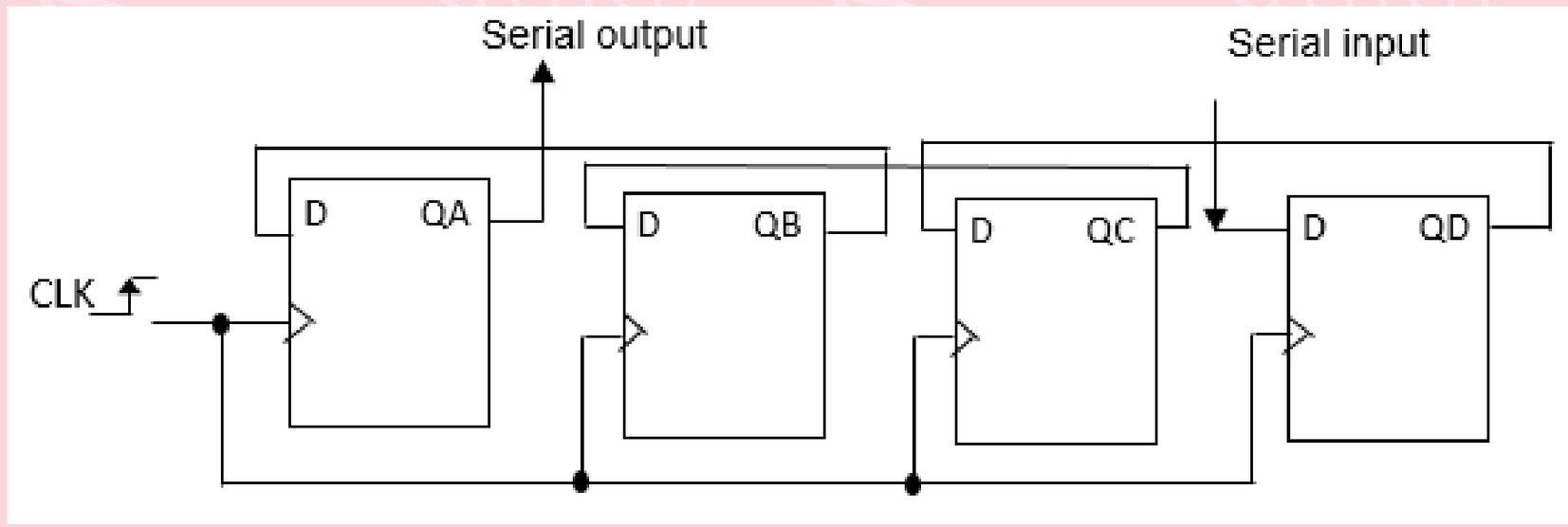
~99~

APPLICATION

ARITHMETIC

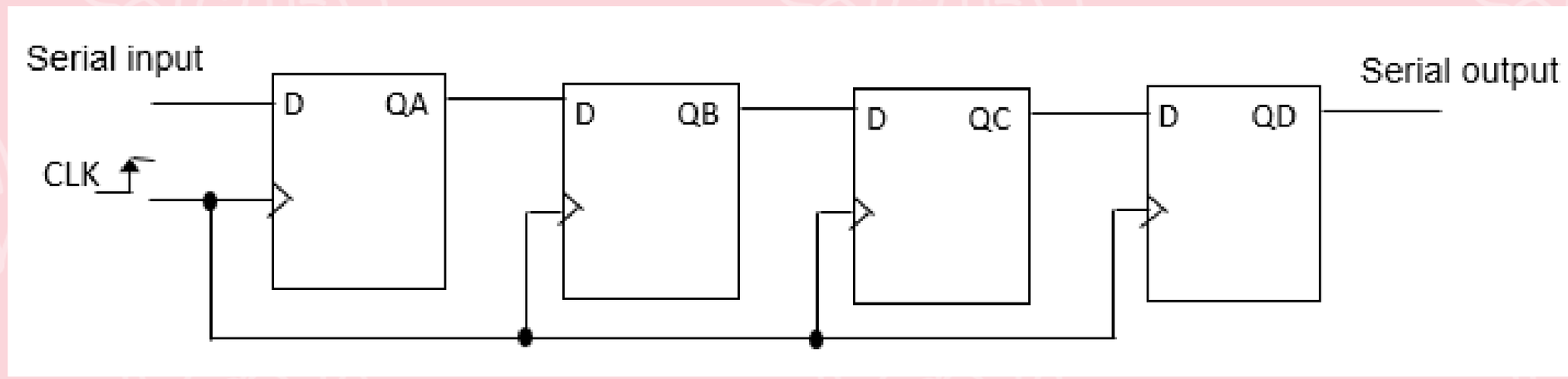
MULTIPLE

shifted from RIGHT to the LEFT



DIVIDER

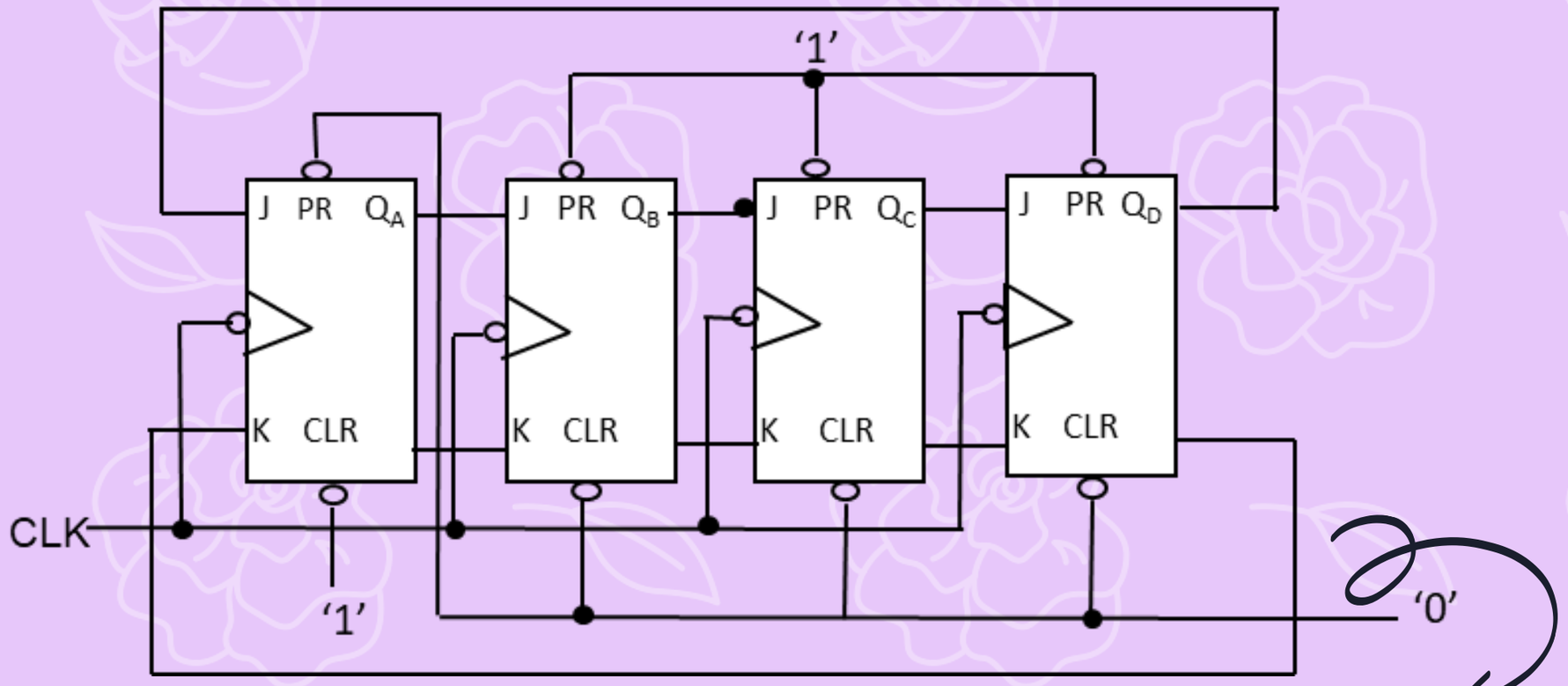
shifted from LEFT to the RIGHT



APPLICATION

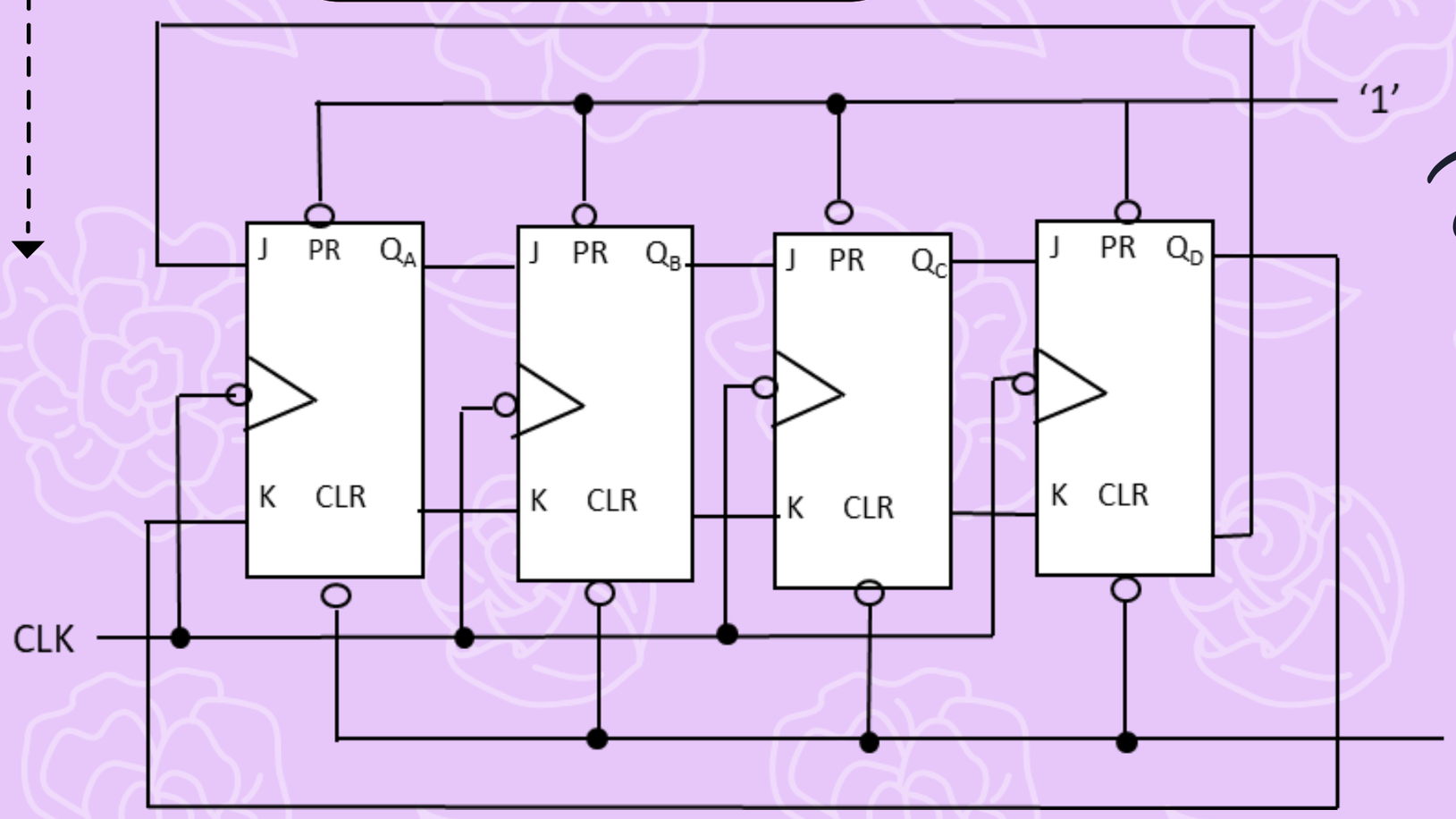
COUNTER

RING COUNTER



A ring counter is a type of counter composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "ring" structure.

JOHNSON COUNTER



A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first.

QUESTION 1

Show **TWO** (2) arithmetic operations that can be performed by shift register with using original decimal number 22 for each operation at least two(2) shift.

QUESTION 2

The content of Johnson counter is initially binary 111011. With the aid of truth table, show how the shift register is used until 7th clock pulse.

QUESTION 3

Use 5-bit serial in - serial out (SISO) concept to complete the table. Input data is 11010 and initial data in flip-flop is 00101.

QUESTION 4

List **FOUR** (4) types of shift register.

QUESTION 5

The content of 5-bit SISO is initially 11001. With the aid of a truth table, visualize the displacement data if new data 10110 is right shifted into the register.

QUESTION 6

The bit sequence 10011 is serially entered into a 5-bit parallel out shift register with an initial data of 10101. Complete the truth table for the data movement.

ANSWER 1

a) Multiple
2nd shift – 01011000

b) Divider
2nd shift – 00000101

ANSWER 2

CLK	Output Series						
	QA	QB	QC	QD	QE	QF	QF′
0	1	1	1	0	1	1	0
1	0	1	1	1	0	1	0
2	0	0	1	1	1	0	1
3	1	0	0	1	1	1	0
4	0	1	0	0	1	1	0
5	0	0	1	0	0	1	0
6	0	0	0	1	0	0	1
7	1	0	0	0	1	0	1

ANSWER 3

CLK	DATA	QA	QB	QC	QD	QE
0		0	0	1	0	1
1	0	0	0	0	1	0
2	1	1	0	0	0	1
3	0	0	1	0	0	0
4	1	1	0	1	0	0
5	1	1	1	0	1	0

ANSWER 4

i. Serial In Serial Out (SISO)
ii. Serial In Parallel Out (SIPO)
iii. Parallel In Serial Out (PISO)
iv. Parallel In Parallel Out (PIPO)

ANSWER 5

CLK	DATA	QA	QB	QC	QD	QE
0		1	1	0	0	1
1	0	0	1	1	0	0
2	1	1	0	1	1	0
3	1	1	1	0	1	1
4	0	0	1	1	0	1
5	1	1	0	1	1	0

ANSWER 6

CLK	DATA	QA	QB	QC	QD	QE
0		1	0	1	0	1
1	1	1	1	0	1	0
2	1	1	1	1	0	1
3	0	0	1	1	1	0
4	0	0	0	1	1	1
5	1	1	0	0	1	1

Notes

Closing

It is hoped that the students can make good use of this e-book. This is because this e-book is compiled using a mind map approach to make it easier for students to master the subject of Digital Electronics. This mind map contains important points related to the subject and the graphic design is also arranged in an interesting arrangement to attract students' interest in mastering the subject of Digital Electronics. At the end of each chapter, the final exam questions of the previous session have also been prepared to enable students to do appropriate exercises and familiarize students with the final exam questions.

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THANK
YOU

POLITEKNIK
MALAYSIA
TUANKU SULTANAH BAHIYAH

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